VITESSE

VSC8211 Datasheet

Single Port 10/100/1000BASE-T, 1000BASE-X, and 100BASE-FX PHY

1 General Description

Ideally suited for Gigabit uplinks on Fast Ethernet switches, Fiber Optics, Media Converter applications, and GBIC/SFP modules, Vitesse's industry-leading low power VSC8211 integrates a high-performance 1.25Gbps SerDes and a triple speed (10/100/1000BASE-T) transceiver, providing unmatched tolerance to noise and cable plant imperfections.

Consuming approximately 700mW, the device requires only 3.3V and 1.2V power supplies. To further minimize system complexity and cost, the VSC8211's twisted pair interface features fully integrated line terminations, exceptionally low EMI, and robust Cable Sourced ESD (CESD) performance.

The VSC8211 provides systems designers with maximum design flexibility, offering direct connectivity to virtually any parallel or serial MAC, optical module, or triple speed GBIC/SFP connector. In addition to the familiar parallel MAC side interfaces (GMII, RGMII, MII, TBI, and RTBI), the device features two serial interfaces to minimize signal overhead: a 1000BASE-X compliant SerDes and SGMII. In 1000BASE-X SerDes mode, the VSC8211 may be used to connect a MAC either to copper media (MAC to Cat-5) or to a 1000BASE-X optical module (MAC-to-Optics). In SGMII mode, the VSC8211 provides a fully compliant, 4 or 6-pin interface to MACs. The 1000BASE-X SerDes and SGMII interfaces offer either automatic or user-controlled auto-negotiation priority resolution between the 1000BASE-X and 1000BASE-T auto-negotiation processes. A single chip copper to optics Media Converter can be easily implemented by simultaneous use of the SerDes and Cat-5 media interfaces. This device also supports 100BASE-FX over its copper media interface.

To minimize power consumption, the VSC8211 offers several programmable power management modes meeting all Wake-on-LAN requirements. The device also supports Vitesse's comprehensive VeriPHY® Cable Diagnostics, offering the system manufacturer and IT administrator with a complete suite of cable plant diagnostics to simplify the manufacture, installation and management of Gigabit-over-copper networks.

2 Features and Benefits

Features	Benefits
• Very low power consumption	• Reduces power supply costs
• Supports PICMG 2.16 and 3.0 Ethernet backplanes at approximately 500mW	• Lowest power mode reduces power supply costs
• Patented line driver with integrated line side termination resistors	• Allows use of simpler magnetic modules with up to 50% cost savings versus competition • Saves over 12 components per port and reduces PCB area & cost by fifty percent
• Flexible MAC interfaces: Serial: SGMII & SerDes Parallel: RGMII & RTBI (2.5V & 3.3V) GMII, MII, TBI	• Serial: Connects to serial MACs or optical modules Supports copper GBIC/SFP modules • Parallel: Connects to virtually any MAC controller
• User-programmable RGMII timing compensation	• Simplifies PCB layout, eliminating PCB trombones
• High performance 1.25Gbps SerDes	• Supports CAT-5, fiber optic, and backplane interfaces from a single device • Suitable for dual media (copper & fiber optics) switch ports, Gigabit uplinks on Fast Ethernet switches, GBICs/SFPs, LOM
• Auto-media Sense detects and configures to support fiber or copper	• Single chip solution for flexible media support

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Features	Benefits
• User-configurable copper or fiber link selection preference with programmable interrupt and signal detect I/O pins	• Ensures plug-n-play link configuration when connected to any copper, fiber, or backplane link partner
• Compliant with IEEE 802.3 (10BASE-T, 100BASE-TX, 1000BASE-T, 1000BASE-X, 100BASE-FX) and SFP MSA specifications	• Ensures seamless deployment throughout copper and optical networks with industry's highest tolerance to noise and substandard cable plants
• Over 150m of Category-5 reach with industry's highest noise tolerance	• Ensures trouble-free deployment in real world Ethernet networks
• Several flexible power management modes	• Reduces power consumption and system costs; fully compliant with Wake-on-LAN requirements
• Small footprint 10mm x 14mm, 117-LBGA package	• Suitable for Gigabit switch ports, GBICs/SFPs, media converters

3 Applications

- Dual Media Switch Ports
- iSCSI and TOE LOM
- Media Converters
- Triple-speed GBIC/SFP modules
- Backplanes

4 Application Diagrams

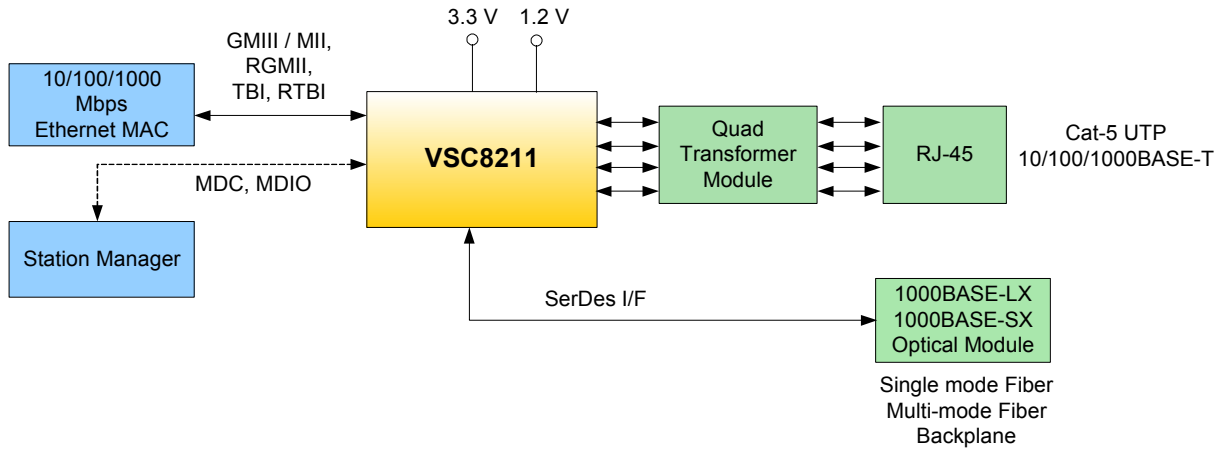


Figure 1. Parallel MAC to Cat-5, Fiber Optics, or Backplanes

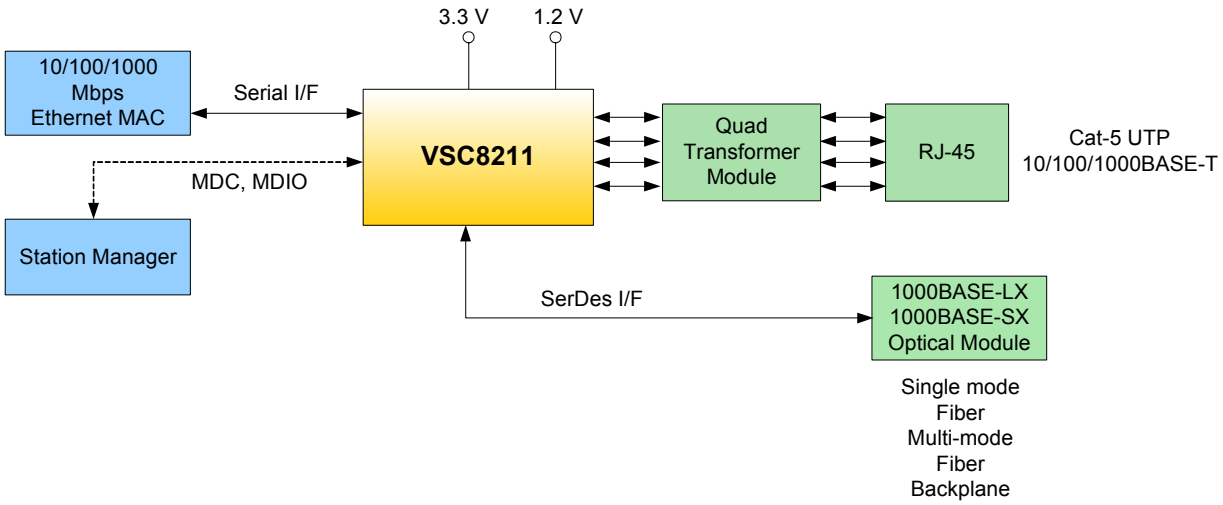


Figure 2. Serial MAC to Cat-5, Fiber Optics, or Backplanes

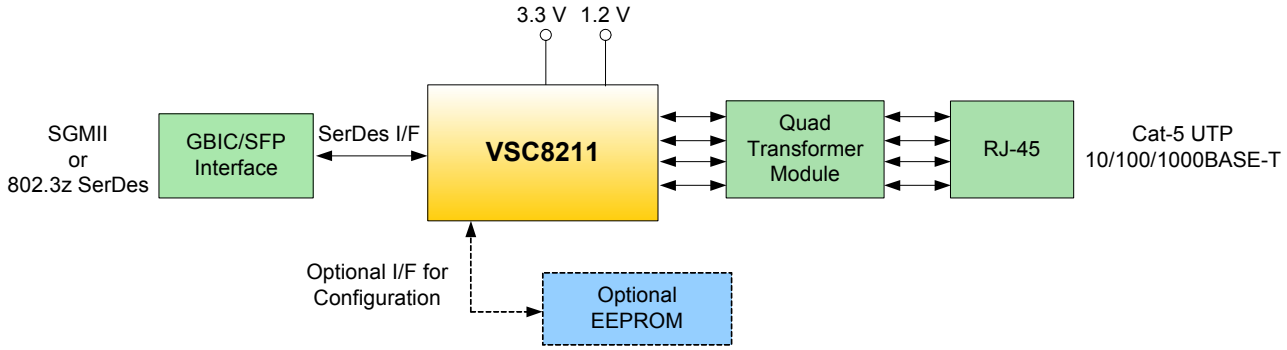
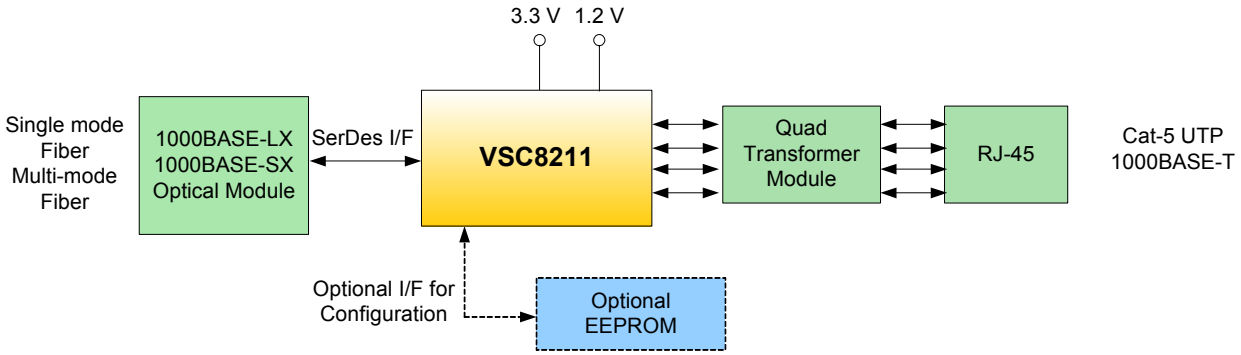


Figure 3. GBIC/SFP Serial Interface (SGMII or 802.3z SerDes to Cat-5)



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5 Relevant Specifications & Documentation

The VSC8211 conforms to the following specifications. Please refer to these documents for additional information.

Specification - Revision	Description
IEEE 802.3-2002	Carrier Sense Multiple Access with Collision Detection (CSMA/CD) Access Method and Physical Layer Specifications. IEEE 802.3-2002 consolidates and supersedes the following specifications: 802.3ab (1000BASE-T), 802.3z (1000BASE-X), 802.3u (Fast Ethernet), with references to ANSI X3T12 TP-PMD standard (ANSI X3.263 TP-PMD).
IEEE 1149.1-1990	Test Access Port and Boundary Scan Architecture[1]. Includes IEEE Standard 1149.1a-1993 and IEEE Standard 1149.1b-1994.
JEDEC EIA/JESD8-5	2.5V±0.2V (Normal Range), and 1.8V to 2.7V (Wide Range) Power Supply Voltage and Interface Standard for Nonterminated Digital Integrated Circuits.
JEDEC JESD22-A114-B	Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM). Revision of JESD22-A114-A.
JEDEC JESD22-A115-A	Electrostatic Discharge (ESD) Sensitivity Testing Machine Model (MM). Revision of EIA/JESD22-A115.
JEDEC EIA/JESD78	IC Latch-Up Test Standard.
MIL-STD-883E	Miltary Test Method Standard for Microcircuits.
Cisco SGMII v1.7	Cisco SGMII specification
RGMII Specification - v2.0	Reduced Pin-Count Interface for Gigabit Ethernet Physical Layer Devices (per Hewlett Packard). Includes both RGMII and RTBI standards.
PICMG 2.16	IP Backplane for CompactPCI.
Advanced TCA™ Base PICMG 3.0	IP Backplane specification for CompactPCI v3.0.
Cisco InLine Power Detection Algorithm	Cisco Systems InLine Power Detection: http://www.cisco.com/en/US/products/hw/phones/ps379/products_tech_note09186a00801189b5.shtml
Small Form-factor Pluggable (SFP) Transceiver MultiSource Agreement	Specification for pluggable fiber optic transceivers. Describes module data access protocol and interface.

[1] Often referred to as the “JTAG” test standard.

6 Datasheet Conventions

Conventions used throughout this datasheet are specified in the following table.

Convention	Syntax	Examples	Description
Register number	RegisterNumber.Bit or RegisterNumber.BitRange	23.10 23.12:10	Register 23 (address 17h), bit 10. Register 23 (address 17h), bits 12, 11, and 10.
Extended Page Register Number[1]	RegisterNumberE.Bit or RegisterNumberE.BitRange	23E.10 23E.12:10	Extended Register 23 (address 17h), bit 10. Extended Register 23 (address 17h), bits 12, 11, and 10.
Signal name (active high)	SIGNALNAME[2]	PLLMODE	Signal name for PLLMODE.
Signal name (active low)	$\overline{\text{SIGNALNAME}}$[2]	$\overline{\text{RESET}}$	Active low reset signal.
Signal bus name	BUSNAME[MSB:LSB][2]	RXD[4:2]	Receive Data bus, bits 4, 3, and 2.

[1] For more information about MII Extended Page Registers, see Section 24: "PHY Register Set Conventions," page 80.
[2] All signal names are in all CAPITAL LETTERS.

7 Document History and Notices

Revision Number	Date	Comments
0.1.0	Feb. 13 04	First Preliminary Release
0.1.1	May 11 04	Updated pin description with VDD12A and Power supply recommendations. Added Errata Section. Updated 'specification' section with VDD12A reference. Updated LED ECO changes. Added GMII,MII,TBI timing sections
2.0	July 08 04	Updated document style to reflect Vitesse corporate standards. Replaced Errata section with Design Guidelines section.
4.0	August 17 05	Added lead-free (Pb-free) package information. Updated register section. Added Reset Timing section.
4.1	October 2006	• In the media converter application diagram, the RJ-45 speed was corrected from 10/100/1000BASE-T to 1000BASE-T. • Throughout the datasheet, information was added regarding the 100BASE-FX mode. The following lists the main information: – For information about twisted pair signals in 100BASE-FX mode, see Table 12: "Twisted Pair Interface Signals". – For information about 100BASE-FX system schematics, see Figure 13: "System Schematic – '100Mbps Fiber Media' Implementation". – For information about 100BASE-FX connections and initialization, see Section 11.5: "100Mbps Fiber Support Over Copper Media Interface" and Section 33.4: "100BASE-FX Initialization Script". – For information about 100BASE-FX current consumption, see Table 43: "VDDIO @ 3.3V, RGMII-100BASE-FX, FDX, 1518 Byte Random data packet, 100% Utilization, SFP Mode Off". • In the list of LED function assignments, the function of LED pin 3, value 00, was corrected from Collision to Link/Activity. • In the listing of JTAG interface instruction codes, the register width given for the instructions EXTEST and SAMPLE/PRELOAD was corrected from 196 bits to 78 bits. • The MII transmit timing diagram was redrawn to more accurately reflect the delay from TXCLK to TXD[3:0], TXEN, and TXER. For more information about this specification, see Figure 39: "MII Transmit AC Timing (100Mbps)". • In the JTAG interface AC timing diagram, missing labels were added that had been left out in the prior revision. • In the reset AC timing diagram, the MDIO signal pulse width was widened to be more accurate relative to the pulse width of the REFCLK signal. For more information about this specification, see Figure 51: "RESET AC Timing". • In the reset AC timing specifications, T_{READY} signal, a condition was added that if EEPROM is present, an additional 100ms is required. For more information about reset AC timing, see Table 73: "RESET AC Timing Specification".

8 Device Block Diagram

The diagram below depicts the primary functional blocks and pins for the VSC8211.

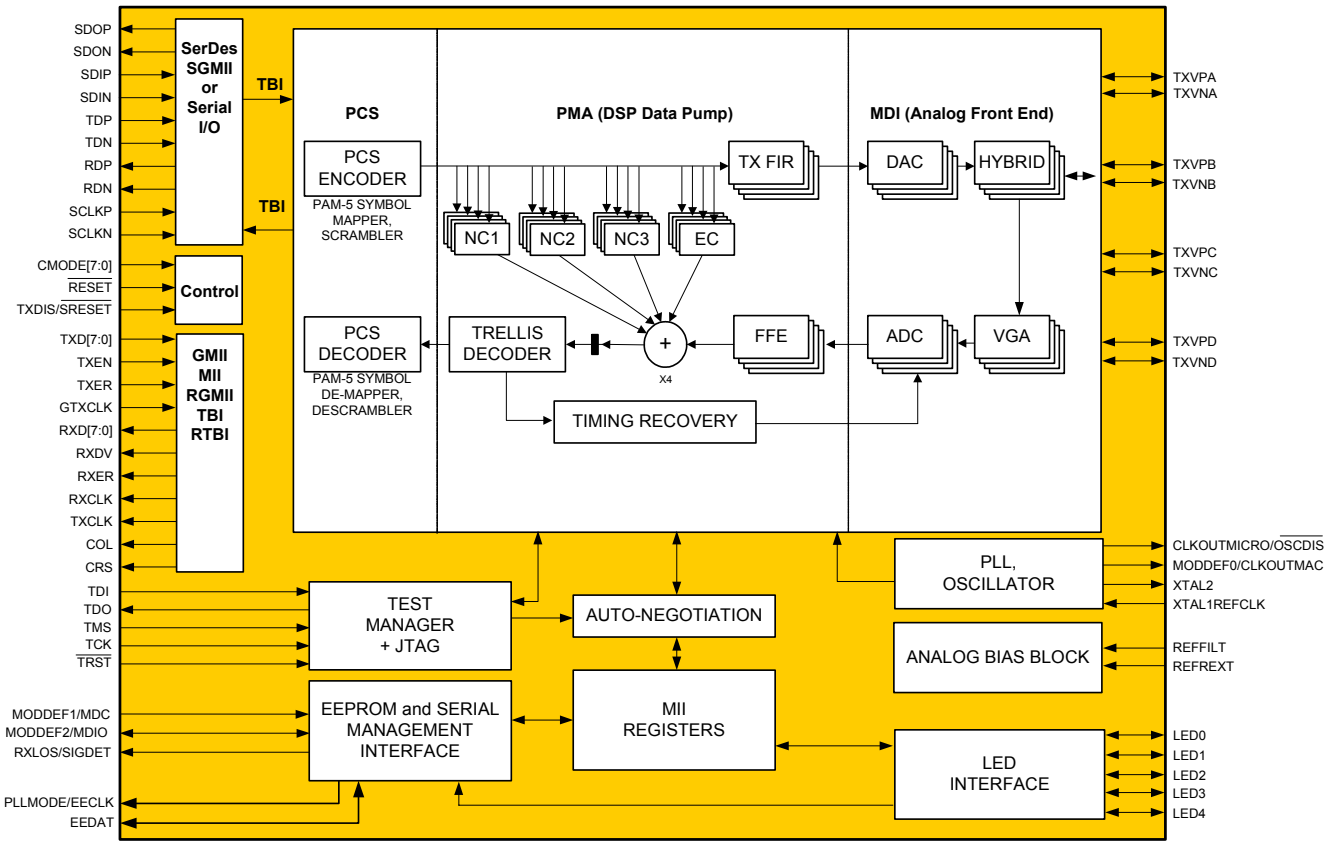
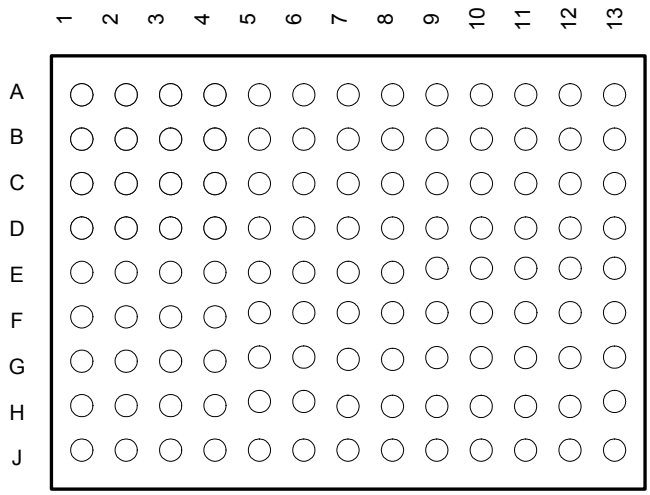


Figure 5. VSC8211 Block Diagram

9 Package Pin Assignments & Signal Descriptions

9.1 VSC8211 117-Ball LBGA Package Ball Diagram

The following diagram shows the view from the top of the package with underlying BGA ball positions superimposed.



1.0 mm Ball Pitch (10 mm x 14 mm body)
(Top View)

Figure 6. VSC8211 117 Ball LBGA Package Ball Diagram

9.2 LBGA Ball to Signal Name Cross Reference[1]

	1	2	3	4	5	6	7	8	9	10	11	12	13	
A	TXEN	GTXCLK	TXCLK	RXER	RXDV	RXD1	RXD3	RXD5	RXD7	MODDEF0/ CLKOUT-MAC	TDI	$\overline{\text{RESET}}$	LED0	A
B	TXD1	TXDO	TXER	COL	RXCLK	RXD0	RXD2	RXD4	RXD6	TMS	TDO	LED1	LED2	B
C	TXD3	TXD2	VDDIOMAC	CRS	VSS	VDDIOMAC	RXLOS/ SIGDET	$\overline{\text{TRST}}$	TCK	VDD12	VDD12	LED3	LED4	C
D	TXD5	TXD4	VDDIOMAC	VSS	VSS	VSS	VSS	VSS	VSS	VDDIOCTRL	CMODE7	CMODE6	CMODE5	D
E	TXD7	TXD6	NC	VSS	VSS	VSS	VSS	VSS	VSS	VSS	CMODE2	CMODE3	CMODE4	E
F	SDON	SDOP	VDD12	VDD12	VSS	VSS	VSS	VSS	VSS	VDD33A	CMODE0	TXVND	TXVPD	F
G	SDIN	SDIP	VDD12	MODDEF2/ MDIO	TXDIS/ $\overline{\text{SRESET}}$	CLKOUT-MICRO/ $\overline{\text{OSCDIS}}$	VDDIO-MICRO	VDD33A	VDD33A	VDD33A	CMODE1	TXVNC	TXVPC	G
H	RDN	RDP	MODDEF1/ MDC	$\overline{\text{MDINT}}$	EEDAT	REFFILT	VDD12A	NC	VSS	XTAL2	VSS	TXVNB	TXVPB	H
J	SCLKP	SCLKN	TDP	TDN	EECLK/ PLLM-ODE	REFREXT	VSS	NC	VSS	XTAL1/ REFCLK	VSS	TXVNA	TXVPA	J
	1	2	3	4	5	6	7	8	9	10	11	12	13	

Figure 7. 117-Ball LBGA Signal Map (top view)

[1]GMII Signal Names are shown for all Parallel MAC Interface Signals, except TXCLK (A3). See Section 9.4.8 on page 26 and Section 9.4.9 on page 28 for Signal Names in other Parallel MAC Interface Modes.

9.3 Signal Type Description

Table 1. Signal Type Description

Symbol	Signal Type	Description
I	Digital Input	Standard digital input signal. No internal pull-up or pull-down.
I_{PU}	Digital Input with Pull-up	Standard digital input. Includes on-chip 100kΩ pull-up to VDDIOMAC, VDDIOMICRO, VDDIOCTRL, or the VDD33A supply. Refer to Section 9.5: "Power Supply and Associated Functional Signals" for details.
I_{PU5V}	Digital Input with Pull-up	Standard digital input. Includes on-chip 100kΩ pull-up to VDDIOMAC, VDDIOMICRO, VDDIOCTRL, or the VDD33A supply. Refer to Section 9.5: "Power Supply and Associated Functional Signals" for details. This input pin is 5V tolerant.
I_{PD}	Digital Input with Pull-down	Standard digital input. Includes on-chip 100kΩ pull-down to GND.
I_{PD5V}	Digital Input with Pull-down	Standard digital input. Includes on-chip 100k Ω pull-down to GND. This input pin is 5V tolerant.
I_{DIFF}	Differential Input Pair	SerDes differential input pair with 100Ω or 150Ω differential terminations. Pins should be AC-coupled with external 0.01µF capacitors.
O	Digital Output	Standard digital output signal.
O_{ZC}	Impedance Controlled Output	50Ω integrated (on-chip) source series terminated, digital output signal. Used primarily for timing-sensitive, high speed MAC I/F and 125MHz clock output pins, in addition to high speed manufacturing test mode pins.
O_{DIFF}	Differential Output Pair	SerDes differential output pair, with on-chip 100Ω or 150Ω differential terminations. Pins should be AC-coupled with external 0.01µF capacitors.
I/O	Digital Bidirectional	Tristate-able, digital input and output signal.
I_{PU}/O	Digital Bidirectional	Tristate-able, digital input and output signal. Includes on-chip 100kΩ pull-up to VDDIOMAC, VDDIOMICRO, VDDIOCTRL, or the VDD33A supply. Refer to Section 9.5: "Power Supply and Associated Functional Signals" for details.
I_{PD}/O	Digital Bidirectional	Tristate-able, digital input and output signal. Includes on-chip 100kΩ pull-down to GND.
OD	Digital Open Drain Output	Open drain digital output signal. Must be pulled to VDDIOMICRO through an external pull-up resistor.
A_{DIFF}	Analog Differential	Analog differential signal pair for twisted pair interface.
A_{BIAS}	Analog Bias	Analog bias or reference signal. Must be tied to external resistor and/or capacitor bias network, as shown in Section 10: "System Schematics".
I_A	Analog Input	Analog input for sensing variable voltage levels.
OS	Open Source	Open source digital output signal. Must be pulled to GND through an external pull-down resistor.
P	Power Supply	Power supply connection. Must be connected to specified power supply plane.
G	GND	Ground Connection. Must be connected to ground.
NC	No Connect	No connect signal. Must be left floating.

9.4 Detailed Pin Descriptions

9.4.1 Configuration and Control Signals

Table 2. Configuration and Control Signals

117 LBGA Ball	Signal Name	Type	Description
D11 D12 D13 E13 E12 E11 G11 F11	CMODE7 CMODE6 CMODE5 CMODE4 CMODE3 CMODE2 CMODE1 CMODE0	I_A	**Hardware Chip Mode Select.** The CMODE inputs are used for hardware configuration of the various operating modes of the PHY. Each pin has multiple settings, each of which is established by an external 1% resistor tied to GND or VDD33A. See Section 19: "Hardware Configuration Using CMODE Pins" for details on configuring the PHY with the CMODE pins.
A12	$\overline{\text{RESET}}$	I	**Hardware Chip Reset.** $\overline{\text{RESET}}$ is an active low input. When asserted, it powers down all of the internal reference voltages and the PLLs. It resets all internal logic, including the DSPs and the MII Management Registers. Hardware reset is distinct from soft reset which only resets the port to accept new configuration based on register settings.
G5	TXDIS/ $\overline{\text{SRESET}}$	I_{PU}	**Transmit Disable or Software Reset.** When asserted, it places the PHY in a low power state, which includes disabling the SerDes interface. Although the device is powered down, non-volatile, Serial Management Interface registers retain their values. TXDIS and $\overline{\text{SRESET}}$ are simply two names for the same function. The assertion state (active high or low respectively) of this input pin is determined by the value of Extended MII Register 21E.15 'SFP MODE' set at startup using Hardware Configuration or via the EEPROM interface. Refer to Section 19: "Hardware Configuration Using CMODE Pins" and Section 20: "EEPROM Interface" for details on configuration at startup.

9.4.2 System Clock Interface Signals (SCI)

Table 3. System Clock Interface Signals (SCI)

117 LBGA BALL	Signal Name	Type	Description
J10	XTAL1/ REFCLK	I	**XTAL1 - Crystal Oscillator Input.** Enabled by pulling OSCDIS (Internal Oscillator Disabled) high, a 25MHz parallel resonant crystal, with a +/- 50ppm frequency tolerance, should be connected across XTAL1 and XTAL2. 33pF capacitors should be connected from XTAL1 and XTAL2 to ground. PLLMODE should be left floating (or pulled low) on reset when a 25MHz crystal is used. **REFCLK - PHY Reference Clock Input.** The reference input clock can either be a 25MHz (PLLMODE is low) or 125MHz (PLLMODE is high) reference clock, with a +/-50ppm frequency tolerance. See EECLK / PLLMODE pin description for more details.
H10	XTAL2	O	**Crystal Output.** 25MHz parallel resonant crystal oscillator output. 33pF capacitors should be connected from both XTAL1 and XTAL2 to ground when using a crystal. PLLMODE should be left floating (or tied low) on reset when using the 25MHz crystal. This output can be left floating if driving XTAL1/REFCLK with a reference clock.
G6	CLKOUTMICRO/ $\overline{\text{OSCDIS}}$	I_{PU}/O	**CLKOUTMICRO - Clock Output.** This is a 4MHz (default) or a 125MHz output clock depending on the value of Extended MII Register 20E.8. The clock output frequency can be set at startup by hardware configuration. Refer to Section 19: "Hardware Configuration Using CMODE Pins" for details. The voltage levels of the clock are based on the VDDIOMICRO power supply. **$\overline{\text{OSCDIS}}$ - Active Low on-chip Oscillator Disable Input.** This input is sampled during the device power-up sequence or on assertion of $\overline{\text{RESET}}$. When sampled high, the PHY enables the internal on-chip oscillator allowing operation with a 25MHz crystal. When sampled low, the PHY's oscillator is turned off and the PHY must be supplied with an external 25MHz or 125MHz clock on the REFCLK pin.
A10	MODDEF0/ CLKOUTMAC	O	The functionality of this signal pin depends on the value for Extended MII Register 21E.15 'SFP Mode' which is set at startup. Refer to Section 19: "Hardware Configuration Using CMODE Pins" and Section 20: "EEPROM Interface" for details on configuration at startup. **MODDEF0 – Active Low PHY Ready Indicator Output (valid in SFP Mode, when MII Register 21E.15 = 1).** This output is driven high immediately on PHY power-up or reset. This signal is asserted low after the PHY startup sequence has completed and the PHY has enabled access to the EEPROM connected to EEPROM Interface through the Serial Management Interface. The minimum time this signal is high before being driven low is 10ms. The maximum time depends on the startup information stored in the EEPROM. Refer to Section 21: "PHY Startup and Initialization" and Section 20: "EEPROM Interface" for details. **CLKOUTMAC – 125MHz Clock Output (valid in IEEE Mode, when MII Register 21E.15 = 0).** The PHY drive a 125MHz clock output after the PHY startup sequence has completed. This clock can be disabled by clearing MII Register 18.0.

9.4.3 Analog Bias Signals

Table 4. Analog Bias Signals

117 LBGA BALL	Signal Name	Type	Description
J6	REFREXT	A_{BIAS}	**REFREXT - Reference External Resistor.** Bias pin connects through external 2kΩ (1%) resistor to analog ground.
H6	REFFILT	A_{BIAS}	**REFFILT - Reference Filter.** Filter internal reference through external 0.1µF (10%) capacitor to analog ground.

9.4.4 JTAG Access Port

Table 5. JTAG Access Port

117 LBGA BALL	Signal Name	Type	Description
A11	TDI	I_{PU5V}	**JTAG Test Data Serial Input Data.** Serial test pattern data is scanned into the device on this input pin, which is sampled with respect to the rising edge of TCK. This pin should be tied high to VDDIOCTRL in designs that do not require JTAG functionality.
B11	TDO	O_{ZC}	**JTAG Test Data Serial Output Data.** Serial test data from the PHY is driven out of the device on the falling edge of TCK. This pin should be left floating during normal chip operation.
B10	TMS	I_{PU5V}	**JTAG Test Mode Select.** This input pin, sampled on the rising edge of TCK, controls the TAP (Test Access Port) controller's 16-state, instruction state machine. This pin should be tied high to VDDIOCTRL in designs that do not require JTAG functionality.
C9	TCK	I_{PU5V}	**JTAG Test Clock.** This input pin is the master clock source used to control all JTAG test logic in the device. This pin should be pulled down with a 2kΩ pull-down resistor in designs that require JTAG functionality. This pin should be tied low in designs that do not require JTAG functionality.
C8	$\overline{TRST}$	I_{PU5V}	**JTAG Reset.** This active low input pin serves as an asynchronous reset to the JTAG TAP controller's state machine. As required by the JTAG standard, this pin includes an integrated on-chip pull-up (to VDDIOCTRL) resistor. Because of the internal pull-up, if the JTAG controller on the printed circuit board does *not* utilize the $\overline{TRST}$ signal, then the device will still function correctly when the $\overline{TRST}$ pin is left unconnected on the board. If the JTAG port of the PHY is not used on the printed circuit board, then this pin should be pulled down with a 2kΩ pull-down resistor or a falling edge must be provided to this pin after PHY power up.

9.4.5 Serial Management Interface Signals

Table 6. Serial Management Interface Signals

117 LBGA BALL	Signal Name	Type	Description
H3	MODDEF1/ MDC	I	The Functionality of this pin is determined by the value of Extended MII Register 21E.15 'SFP MODE' set at startup using CMODE Hardware Configuration or via the EEPROM interface. **MODDEF1 - Serial MSA Clock (valid in SFP Mode, when MII Register 21E.15 = 1).** MODDEF1 is the clock input of the two-wire serial interface for accessing the PHY's registers or the EEPROM connected to the EEPROM Interface using the protocol specified in the MSA specification. Although typically operated at 100kHz, MODDEF1 can be operated at a maximum of 1MHz. **MDC - Management Data Clock (valid in IEEE Mode, when MII Register 21E.15 = 0).** MDC is the clock input of the two wire serial interface for accessing the PHY's registers or the EEPROM connected to the EEPROM Interface using the Serial Management Interface protocol specified in the IEEE 802.3 specification. This clock is typically between 0 to 12.5MHz and is usually asynchronous with respect to the PHY's transmit or receive clock.
G4	MODDEF2/ MDIO	I/O	The Functionality of this pin is determined by the value of Extended MII Register 21E.15 'SFP MODE' set at startup using CMODE Hardware Configuration or via the EEPROM interface. **MODDEF2 - Serial I/O Data (valid in SFP Mode, when MII Register 21E.15 = 1).** MODDEF2 is the data line of the two-wire serial interface for accessing the PHY's registers or the EEPROM connected to the EEPROM Interface using the protocol specified in the MSA specification. This pin normally requires a 1.5kΩ to 4.7kΩ pull-up resistor to VDDIOMICRO at the Station Manager. The value of the pull-up resistor depends on the MODDEF1 frequency and the capacitive load on the MODDEF2 line. **MDIO - Serial I/OP Data (valid in IEEE Mode, when MII Register 21E.15 = 0)**. MDIO is the data line of the two-wire serial interface for accessing the PHY's registers or the EEPROM connected to the EEPROM Interface using the Serial Management Interface protocol specified in the IEEE 802.3 specification. This pin normally requires a 1.5kΩ to 4.7kΩ pull-up resistor to VDDIOMICRO at the Station Manager. The value of the pull-up resistor depends on the MDC frequency and the capacitive load on the MDIO line.
H4	$\overline{\text{MDINT}}$	OD	**Management Data Interrupt.** $\overline{\text{MDINT}}$ is asserted whenever there is a change in operating status of the device. This open drain signal indicates a change in the PHY's link operating conditions for which a Station Manager must interrogate to determine further information. See MII Register 25 and MII Register 26 for more information. The assertion polarity of the $\overline{\text{MDINT}}$ is determined by the presence of a pull-up or pull-down on the $\overline{\text{MDINT}}$ pin. If the $\overline{\text{MDINT}}$ pin is pulled up to VDDIOMICRO using a 4.7kΩ to 10kΩ resistor, is becomes an active low signal. If the $\overline{\text{MDINT}}$ pin is pulled down using a 4.7kΩ to 10kΩ resistor, then it becomes an active high signal.

9.4.6 EEPROM Interface Signals

Table 7. EEPROM Interface Signals

117 LBGA BALL	Signal Name	Type	Description
J5	EECLK/ PLLMODE	O_{ZC}/I_{PD}	**EECLK - EEPROM Clock Output.** This output is the clock line of the two-wire, MSA compliant serial EEPROM Interface. This should be connected to the SCL input pin of the AT24 series of Atmel EEPROMs. Refer Section 20: "EEPROM Interface" for details. **PLLMODE - PLL Mode Select Input.** PLLMODE is sampled during the device power-up sequence or on reset. When PLLMODE is high, the PHY expects a 125MHz clock input as the PHY's reference clock. When low (default), a reference clock of 25MHz is expected at the REFCLK pin from either an external crystal or a clock reference. This pin is internally pulled down with a 100kΩ resistor.
H5	EEDAT	O_{ZC}/I_{PD}	**EEPROM Serial I/O Data.** This bidirectional signal is the data line of the two wire, MSA compliant, serial EEPROM Interface. This should be connected to the SDA pin of the AT24 series of Atmel EEPROMs. Refer to Section 20: "EEPROM Interface" for details. The PHY determines that an external EEPROM is present by monitoring the EEDAT pin at power-up or when $\overline{\text{RESET}}$ is de-asserted. If EEDAT has a 4.7kΩ - 10kΩ external pull-up (to VDDIOMICRO) resistor, it assumes an EEPROM is present. The EEDAT pin can be left floating or grounded to indicate no EEPROM.

9.4.7 LED Interface Signals

Table 8. LED Interface Signals

117 LBGA BALL	Signal Name	Type	Description
C13 C12 B13 B12 A13	LED4 LED3 LED2 LED1 LED0	O_{ZC}	**LED - Direct-Drive LED Outputs.** After reset, these pins serve as the direct drive, low EMI, LED driver output pins. All LEDs are active-low and driven at a 3.3V logic-high through the VDD33A analog power supply. The function of each LED can be set using hardware configuration or via MII Register 27. Refer to Section 19: "Hardware Configuration Using CMODE Pins" and MII Register 27 for details.

9.4.8 Parallel MAC Interface Signals - Transmit Signals

The following signals are used in Parallel MAC Interface PHY Operating modes and connect to the parallel data bus MAC via the industry-standard GMII, RGMII, TBI, RTBI and MII interfaces. If these parallel interfaces are not used, all of the following pins may be left unconnected or tied to ground.

Table 9. Parallel MAC Interface Signals - Transmit Signals

117 LBGA BALL	Signal Name Parallel MAC Interface Modes					Type	Description
	TBI	RTBI	GMII	MII	RGMII		
C1 C2 B1 B2	TX[3:0]	TD[8:5] and TD[3:0]	TXD[3:0]	TXD[3:0]	TD[7:4] and TD[3:0]	I_{PD}	**Transmit Data Inputs (All modes).** Transmit code-group data is input on these pins synchronously to the rising edge of GTXCLK in GMII mode and PMATXCLK in TBI mode. Transmit code-group data is input on these pins synchronously to the rising edge and falling edge of TXC in RTBI and RGMII modes. **Multiplexed Transmit Data Nibbles (RTBI mode).** Bits [3:0] are synchronously input on the rising edge of TXC, and bits [8:5] on the falling edge of TXC. **Multiplexed Transmit Data Nibbles (RGMII mode).** Bits [3:0] are synchronously input on the rising edge of TXC, and bits [7:4] on the falling edge of TXC.
E1 E2 D1 D2	TX[7:4]	Not used	TXD[7:4]	Not used	Not used	I_{PD}	**Transmit Data Inputs (TBI mode).** Transmit code-group data is input on these pins synchronously to the rising edge of PMATXCLK in TBI mode. **Transmit Data Inputs (GMII mode).** Transmit code-group data is input on these pins synchronously to the rising edge of GTXCLK in GMII mode.
A1	TX[8]	Not used	TXEN	TXEN	Not used	I_{PD}	**Transmit Data Input (TBI mode).** Transmit code-group data bit 8 is input on this pin synchronously to the rising edge of PMATXCLK in TBI mode. **Transmit Enable Input (GMII, MII modes).** Synchronized to the rising edge of GTXCLK (1000Mb mode) or TXCLK (100Mb mode), this input indicates valid data is present on the TXD bus.

Table 9. Parallel MAC Interface Signals - Transmit Signals *(continued)*

117 LBGA BALL	Signal Name Parallel MAC Interface Modes					Type	Description
	TBI	RTBI	GMII	MII	RGMII		
B3	TX[9]	TD[9] and TD[4]	TXER	TXER	TXCTL	I_{PD}	**Transmit Data Input (TBI mode).** Transmit code-group data bit 9 is input on this pin synchronously to the rising edge of PMATXCLK in TBI mode. **Multiplexed Transmit Data Input (RTBI mode).** Bit [4] is synchronously input on the rising edge of TXC, and bit [9] on the falling edge of TXC. **Transmit Error Input (GMII, MII modes).** When asserted, this synchronous input causes error symbols to be transmitted from the PHY when operating in 100Mb or 1000Mb modes. **Transmit Enable, Transmit Error Multiplexed Input (RGMII mode).** In RGMII mode, this input is sampled by the PHY on opposite edges of TXC to indicate two transmit conditions of the MAC: 1) on the rising edge of TXC, this input serves as TXEN, indicating valid data is available on the TD input data bus. 2) on the falling edge of TXC, this input signals a transmit error from the MAC, based on a logical derivative of TXEN and TXER, per RGMII specification Version 1.2a, Section 3.4.
A2	PMAT XCLK	TXC	GTXCLK	Not used[1]	TXC	I_{PD}	**PMA Transmit Code Group Clock Input (TBI mode).** 125 MHz transmit code-group clock. This code-group clock is used to latch data into the PMA (in this case, the PHY) for transmission. **Transmit Clock Input (GMII mode).** The transmit clock GTXCLK is a 125MHz, +/-100ppm reference clock used to synchronize the TXD data code group, TXD[7:0], into the PHY. **Transmit Clock Input (RGMII/RTBI mode).** The transmit clock shall be either a 125MHz or 25MHz (for 1000Mb or 100Mb modes, respectively), with a +/-50ppm tolerance.

[1] See TX_CLK pin description in following section.

9.4.9 Parallel MAC Interface Signals - Receive Signals

The following signals are used in Parallel MAC Interface PHY Operating modes and connect to the parallel data bus MAC via the industry-standard GMII, RGMII, TBI, RTBI and MII interfaces. If these parallel interfaces are not used, all of the following pins may be left unconnected or tied to ground.

All output pins in the Parallel MAC interface include impedance-calibrated, tristateable output drive capability.

Table 10. Parallel MAC Interface Signals - Receive Signals

117 LBGA BALL	Signal Name Parallel MAC Interface Modes					Type	Description
	TBI	RTBI	GMII	MII	RGMII		
A7 B7 A6 B6	RX[3:0]	RD[8:5] and RD[3:0]	RXD[3:0]	RXD[3:0]	RD[7:4] and RD[3:0]	O_{ZC}	**Receive Data Code Group (TBI mode).** Bits [3:0] of 10-bit parallel receive code-group data. When code groups are properly aligned, any received code group containing a comma is clocked by the rising edge of PMARXCLK1. **Multiplexed Receive Data Nibbles (RTBI mode).** The MAC synchronously inputs Bits [3:0] on the rising edge of RXC, and bits [8:5] on the falling edge of RXC. **Receive Data Code Group (GMII and MII modes).** Receive data is driven out of the device synchronously to the rising edge of RXC. RXD[3] is the MSB, RXD[0] is the LSB. **Multiplexed Receive Data Nibble (RGMII mode).** Bits [3:0] are synchronously output on the rising edge of RXC, and bits [7:4] on the falling edge of RXC. RXD[3] is the MSB, RXD[0] is the LSB.
A9 B9 A8 B8	RX[7:4]	Leave pins uncon-nected	RXD[7:4]	Leave pins uncon-nected	Leave pins uncon-nected	O_{ZC}	**Receive Data Code Group (TBI mode).** Bits [7:4] of 10-bit parallel receive code-group data. When code groups are properly aligned, any received code group containing a comma is clocked by the rising edge of PMARXCLK1. **Receive Data Code Group (GMII mode).** Receive data is driven out of the device synchronously to the rising edge of RXC. RXD[7] is the MSB.
B5	PMARX CLK0	RXC	RXCLK	RXCLK	RXC	O_{ZC}	**PMA Receiver Clock 0 Output (TBI mode).** The protocol device (MAC) uses the rising edge of this 62.5MHz receive clock to latch in odd-numbered code groups on the received PHY bit stream. This clock may be stretched during code-group alignment and is not shortened. **Receive Clock Output (GMII, MII, RGMII and RTBI modes).** Receive data is sourced from the PHY synchronous to the rising edge of RXCLK in GMII/MII modes or RXC in RGMII/RTBI modes. This clock is recovered from the media.

Table 10. Parallel MAC Interface Signals - Receive Signals *(continued)*

117 LBGA BALL	Signal Name Parallel MAC Interface Modes					Type	Description
	TBI	RTBI	GMII	MII	RGMII		
A3	PMARX CLK1	Leave pins uncon-nected	Leave pins uncon-nected	TXCLK	Leave pins uncon-nected	O_{ZC}	**PMA Receiver Clock 1 Output (TBI mode).** The protocol device (MAC) uses the rising edge of this 62.5MHz receive clock to latch even-numbered code groups on the received PHY bit stream. PMARXCLK1 is 180° out of phase with PMARXCLK0. This clock may be stretched during code-group alignment and is not shortened. **Transmit Clock (MII mode).** 25MHz (100Mb mode) or 2.5MHz (10Mb mode) MII clock output. The MAC uses the rising edge of this clock to synchronize TXD data.
A5	RX[8]	Leave pins uncon-nected	RXDV	RXDV	Leave pins uncon-nected	O_{ZC}	**Receive Data Code Group, bit [8] (TBI mode).** Bit [8] of 10-bit parallel receive code-group data. When code groups are properly aligned, any received code group containing a comma is clocked by the rising edge of PMARXCLK1. **Receive Data Valid Output (GMII, MII modes).** RXDV is asserted by the PHY to indicate that the PHY is presenting recovered and decoded data on the RXD pins. RXDV is synchronous with respect to RXCLK.
A4	RX[9]	RD[9] and RD[4]	RXER	RXER	RXCTL	OZC	**Receive Data Code Group, bit [9] (TBI mode).** Bit [9] of 10-bit parallel receive code-group data. When code groups are properly aligned, any received code group containing a comma is clocked by the rising edge of PMARXCLK1. **Multiplexed Receive Data Nibbles (RTBI mode).** The MAC synchronously inputs Bit [4] on the rising edge of RXC, and bit [9] (MSB) on the falling edge of RXC. **Receiver Error Output (GMII, MII modes).** This active high output is synchronous to the rising edge of the received data clock (RXCLK or RXC). For 1000Mb mode, this signal is asserted when error symbols or carrier extension symbols are received. In 100Mb mode, it is asserted when error symbols are received. **Multiplexed Receive Data Valid / Receive Error Output (RGMII mode).** In RGMII mode, this output is sampled by the MAC on opposite edges of RXC to indicate two receive conditions from the PHY: 1) on the rising edge of RXC, this output serves as RXDV. When high it signals valid data is available on the RD input data bus. 2) on the falling edge of RXC, this output signals a receive error from the PHY, based on a logical derivative of RXDV and RXER, per RGMII specification Version 1.2a, Section 3.4.

Table 10. Parallel MAC Interface Signals - Receive Signals *(continued)*

117 LBGA BALL	Signal Name Parallel MAC Interface Modes					Type	Description
	TBI	RTBI	GMII	MII	RGMII		
C4	COM-DET	Leave pins uncon-nected	CRS	CRS	Leave pins uncon-nected	O_{ZC}	**Comma Detect Output (TBI mode).** A high on this signal indicates that the code-group associated with the current PMARXCLK1 contains a valid comma. In TBI mode, the PHY detects and code-group-aligns to the comma+ bit sequence. **Carrier Sense Output (GMII, MII modes).** Valid only in GMII and MII half duplex modes, CRS is asserted high when a valid carrier is detected on the media.
B4	RXCLK 125	Leave pins uncon-nected	COL	COL	Leave pins uncon-nected	O_{ZC}	**Collision Detect Output (GMII, MII modes).** This output is asserted high when a collision is detected on the media. For full-duplex modes, this output is always low. **Receiver Clock 125MHz Output (TBI mode).** This signal behaves differently, depending on whether TBI loopback mode is enabled: 1) When TBI loopback mode is enabled, RXCLK125 becomes one-half the frequency of the GTXCLK input clock from the protocol device (or MAC). 2) When no carrier is present on the media, this signal is the same as the device's free running output clock signal, CLKOUTMAC. 3) When a valid carrier is detected on the media, this output signal is the recovered clock from the TBI's data stream. When switching from one of these three operating modes to another, RXCLK125's low time will be extended, if necessary, to avoid clock glitching.

9.4.10 Serial MAC/Media Interface Signals

Table 11. Serial MAC/Media Interface Signals

117 LBGA BALL	Signal Name	Type	Description
J3 J4	TDP TDN	I_{DIFF}	**Transmitter Data Differential Input Pair (used in SerDes/SGMII to CAT5 and Parallel MAC to SerDes/AMS PHY Operating Modes).** Differential 1.25Gbaud receiver inputs with register selectable on-chip 100Ω or 150Ω differential termination. The TDP and TDN signals should be AC-coupled with external 0.01µF series capacitors. See Section 10: "System Schematics" for further information.
H2 H1	RDP RDN	O_{DIFF}	**Receiver Data Differential Output Pair (used in SerDes/SGMII to CAT5 and Parallel MAC to SerDes/AMS PHY Operating Modes).** Differential 1.25Gbaud transmitter outputs. External 0.01µF AC coupling capacitors should be located on the PHY side. The register selectable 100Ω or 150Ω differential termination should be placed near the MAC side. See Section 10: "System Schematics" for further information. For information about adjusting the output swing of these pins, see Register 17E (11h) – SerDes Control Register, page 124.

Table 11. Serial MAC/Media Interface Signals *(continued)*

117 LBGA BALL	Signal Name	Type	Description
J1 J2	SCLKP SCLKN	O_{DIFF}	**SGMII Clock Differential Output Pair (used in SGMII to CAT5/SerDes/AMS PHY Operating Modes).** This signal pair is a differential 625MHz SGMII clock for the SGMII data in accordance with Cisco's SGMII specification. These pins should be AC-coupled with external 0.01µF series capacitors or left unconnected when not used. See Section 10: "System Schematics" for further information. For information about adjusting the output swing of these pins, see Register 17E (11h) – SerDes Control Register, page 124.
G2 G1	SDIP SDIN	I_{DIFF}	**Fiber Transceiver Differential Input Pair (used in SGMII to SerDes PHY Operating Modes).** Differential 1.25Gbaud receiver inputs with register selectable on-chip 100Ω or 150Ω differential termination. The SDIP and SDIN signals should be AC-coupled with external 0.01µF series capacitors. These signals usually connect to the RX signals of the Fiber Optic Transceiver or the RX signals of a SerDes over the Backplane.
F2 F1	SDOP SDON	O_{DIFF}	**Fiber Transceiver Differential Output Pairs (used in SGMII to SerDes PHY Operating Modes).** Differential 1.25Gbaud transmitter outputs. The SDOP and SDON signals should be AC-coupled with external 0.01µF AC series capacitors, placed on the PHY side of these traces. These signals usually connect to the TX signals of the Fiber Optic Transceiver or the TX signals of a SerDes over the Backplane. The register selectable 100Ω or 150Ω differential termination should be placed near the Transceiver/SerDes. For information about adjusting the output swing of these pins, see Register 20E (14h) – Extended PHY Control Register #3, page 126.

Table 11. Serial MAC/Media Interface Signals *(continued)*

117 LBGA BALL	Signal Name	Type	Description
C7	RXLOS/ SIGDET	I/O	The functionality of this signal pin depends on the value for Extended MII Register 21E.15 'SFP Mode' which is set at startup. Refer to Section 19: "Hardware Configuration Using CMODE Pins" and Section 20: "EEPROM Interface" for details on configuration at startup. **RXLOS - Receiver Loss of Signal Output (valid in SFP Mode, when MII Register 21E.15 = 1).** This active high signal is asserted when the CAT5 link goes down. The pulse width of the RXLOS signal is configurable. Refer to MII Register 30.1:0 for details. **SIGDET - SerDes Signal Detect (I/O) (valid in IEEE Mode, when MII Register 21E.15 = 0).** SIGDET can be configured as an input or output and can be configured to function as active low or active high at startup using hardware configuration or the EEPROM interface. Refer to Section 19: "Hardware Configuration Using CMODE Pins" or Section 20: "EEPROM Interface" for details on configuration at startup. SIGDET as Input: When used as an input, the SIGDET signal is meant to be connected to the signal detect output of the fiber optic transceiver. If SIGDET is high, this indicates receive activity on the fiber optic transceiver. In input mode, SIGDET is relevant only in the following PHY Operating modes: • Parallel MAC to Fiber (MII Register 23.15:12,23.2:1 = 0xx101) • Parallel MAC to Auto Media Sense (MII Register 23.15:12,23.2:1 = 00x0xx) • Serial to CAT5 (MII Register 23.15:12,23.2:1 = 1xxxxx) If SIGDET is not used as an input, the PHY internally generates the signal detect function, from the incoming data on the TDP and TDN signal pins. SIGDET as Output: For Fiber media, the SIGDET behavior depends upon the input signal levels on the TDP/ TDN pins and is defined as: • If the input signal amplitude is > 200mV peak-to-peak, SIGDET is asserted. • If the input signal amplitude is <200mV, but >50mV, SIGDET is undefined. • If the input signal amplitude is < 50mV peak-to-peak, SIGDET is deasserted. For Serial MAC to CAT5 Media PHY Operating modes, SIGDET is asserted if the CAT5 link has been established. In Parallel MAC to CAT5 Media PHY Operating Modes, SIGDET is always deasserted.

9.4.11 Twisted Pair Interface Signals

Table 12. Twisted Pair Interface Signals

117 LBGA BALL	Signal Name	Type	Description
J13	TXVPA	A_{DIFF}	**TX/RX Channel "A" Positive Signal.** Positive differential signal connected to the positive primary side of the transformer. This signal forms the positive signal of the "A" data channel. In 10/100/1000Mbps mode, this signal generates the secondary side signal, normally connected to RJ-45 pin 1. In 100BASE-FX mode, it is connected instead to the positive SFP transmit data signal (SFP_TD+). See Section 10: "System Schematics" for details.
J12	TXVNA	A_{DIFF}	**TX/RX Channel "A" Negative Signal.** Negative differential signal connected to the negative primary side of the transformer. This signal forms the negative signal of the "A" data channel. In 10/100/1000Mbps mode, this signal generates the secondary side signal, normally connected to RJ-45 pin 1. In 100BASE-FX mode, it is connected instead to the negative SFP transmit data signal (SFP_TD–). See Section 10: "System Schematics" for details.
H13	TXVPB	A_{DIFF}	**TX/RX Channel "B" Positive Signal.** Positive differential signal connected to the positive primary side of the transformer. This signal forms the positive signal of the "B" data channel. In 10/100/1000Mbps mode, this signal generates the secondary side signal, normally connected to RJ-45 pin 1. In 100BASE-FX mode, it is connected instead to the positive SFP receive data signal (SFP_RD+). See Section 10: "System Schematics" for details.
H12	TXVNB	A_{DIFF}	**TX/RX Channel "B" Negative Signal.** Negative differential signal connected to the negative primary side of the transformer. This signal forms the negative signal of the "B" data channel. In 10/100/1000Mbps mode, this signal generates the secondary side signal, normally connected to RJ-45 pin 1. In 100BASE-FX mode, it is connected instead to the negative SFP receive data signal (SFP_RD–). See Section 10: "System Schematics" for details.
G13	TXVPC	A_{DIFF}	**TX/RX Channel "C" Positive Signal.** Positive differential signal connected to the positive primary side of the transformer. This signals forms the positive signal of the "C" data. In 1000Mb mode, this signal generates the secondary side signal, normally connected to RJ-45 pin 4 (not used in 10M/100M modes). See Section 10: "System Schematics" for details.
G12	TXVNC	A_{DIFF}	**TX/RX Channel "C" Negative Signal.** Negative differential signal connected to the negative primary side of the transformer. This signal forms the negative signal of the "C" data channel. In 1000Mb mode, this signal generates the secondary side signal, normally connected to RJ-45 pin 5 (not used in 10M/100M modes). See Section 10: "System Schematics" for details.
F13	TXVPD	A_{DIFF}	**TX/RX Channel "D" Positive Signal.** Positive differential signal connected to the positive primary side of the transformer. This signal forms the positive signal of the "D" data channel. In 1000Mb mode, this signal generates the secondary side signal, normally connected to RJ-45 pin 7 (not used in 10M/100M modes). See Section 10: "System Schematics" for details.
F12	TXVND	A_{DIFF}	**TX/RX Channel "D" Negative Signal.** Negative differential signal connected to the negative primary side of the transformer. This signal forms the positive signal of the "D" data channel. In 1000Mb mode, this signal generates the secondary side signal, normally connected to RJ-45 pin 8 (not used in 10M/100M modes). See Section 10: "System Schematics" for details.

9.4.12 Power Supply and Ground Connections

Table 13. Power Supply and Ground Connections

117 LBGA BALL	Supply Name	Recommended PCB Power Plane	Type	Nominal Supply Voltage (V)	Description
Digital I/O Power Supply Pins					
C6, C3, D3	VDDIOMAC[1]	V+IO	P	3.3V or 2.5V	Power for the Parallel MAC Interface
G7	VDDIOMICRO[1]	V+IO	P	3.3V or 2.5V	Power for SMI and EEPROM Interface
D10	VDDIOCTRL[1]	V+IO	P	3.3V or 2.5V	Power for JTAG I/O
Digital Core Power Supply Pins					
C10, C11, F3, F4, G3[2]	VDD12	V+12	P	1.2V	Power for internal digital logic, and SerDes/ SGMII I/O Power
Analog Power Pins					
F10, G10,G9,G8	VDD33A	V+33A	P	3.3V	Power for MDI, CMODE, PLL, and LED blocks.
H7	VDD12A	V+12A	P	1.2V	Power of PLL and ADC blocks.
Ground Pins					
C5, D4, D5, D6, D7, D8, D9, E4, E5, E6, E7, E8, E9, E10, F5, F6, F7, F8, F9, J7, H9, J9, H11, J11	VSS	GND	G	0V	Ground for all blocks

[1] The I/O power supplies on the PHY are separated on the chip itself to facilitate support for different VDDIO supply voltages. These VDDIO supplies can be run independently at 2.5v or 3.3v I/O.

[2] All these pins must be connected to VDD12 supply.

9.4.13 No Connects

Table 14. No Connects

117 LBGA BALL	Signal Name	Type	Description
E3, H8, J8	NC	NC	**No Connect - must be left floating**

9.5 Power Supply and Associated Functional Signals

Table 15. Power Supply and Associated Functional Signals

Power Supply Pins	Nominal Voltages	Associated Functional Pins
VDDIOMAC	3.3V or 2.5V	RXLOS/SIGDET, RXD[7:0], RXDV, RXER, RXCLK, COL, CRS, TXCLK, TXER, GTX-CLK, TXEN, TXD[7:0], MODDEF0/CLKOUTMAC
VDDIOMICRO	3.3V or 2.5V	EECLK/PLLMODE, EEDAT, TXDIS/$\overline{\text{SRESET}}$, $\overline{\text{MDINT}}$, MODDEF1/MDC, MODDEF2/MDIO, CLKOUTMICRO/$\overline{\text{OSCDIS}}$
VDDIOCTRL	3.3V or 2.5V	$\overline{\text{RESET}}$, TDO, TDI, TMS, TCK, $\overline{\text{TRST}}$
VDD33A	3.3V	LED[4:0], CMODE[7:0], TXVND, TXVPD, TXVNC, TXVPC, TXVNB, TXVPB, TXVNA, TXVPAXTAL2, XTAL1/REFCLK, REFFILT, REFREXT
VDD12	1.2V	RDP, RDN, TDP, TDN, SCLKP, SCLKN, SDIN, SDIP, SDOP, SDON
VDD12A	1.2V	

10 System Schematics

10.1 Parallel Data MAC to CAT5 Media PHY Operating Mode

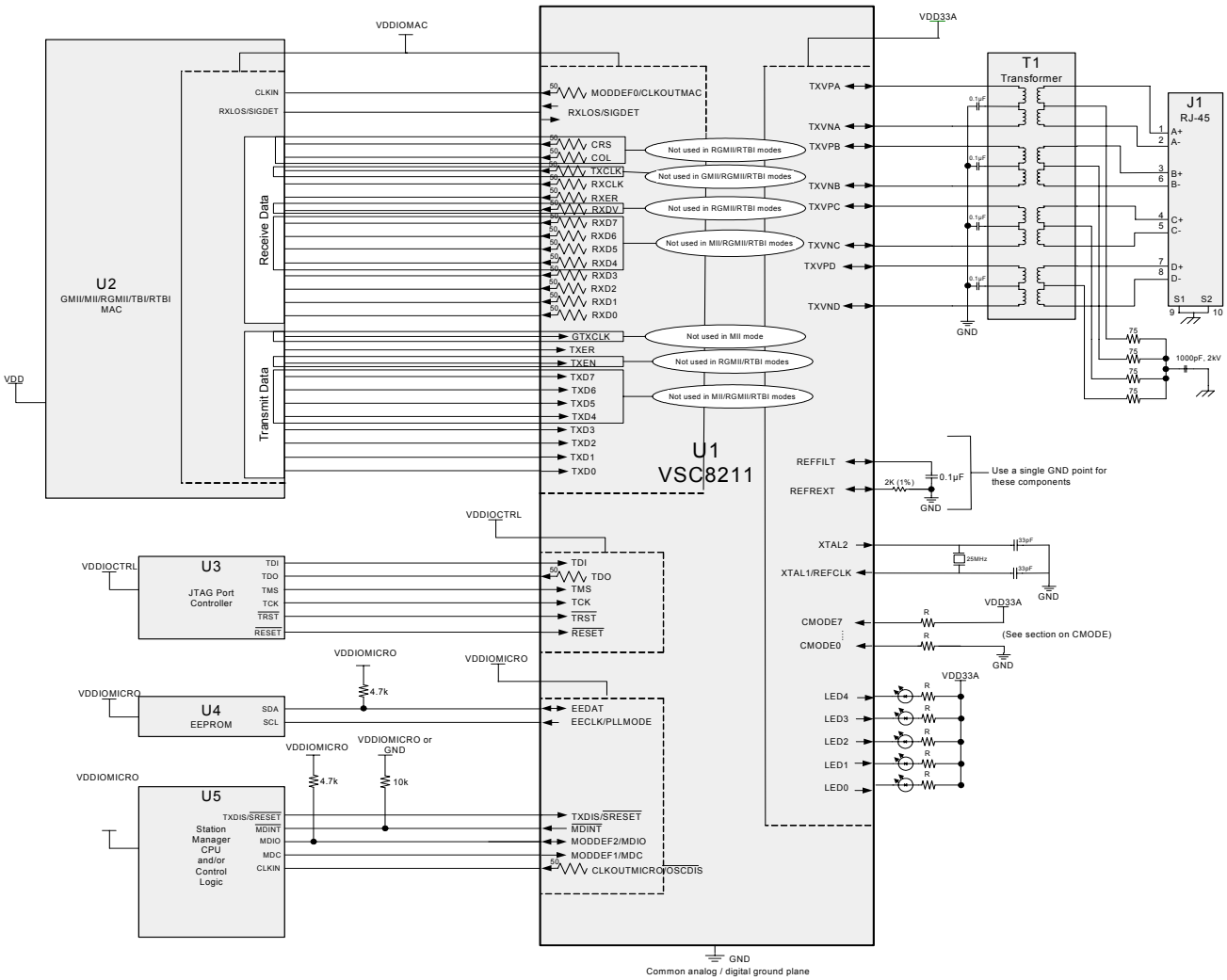


Figure 8. System Schematic – 'Parallel Data MAC to CAT5 Media' PHY Operating Mode

10.2 Parallel Data MAC to 1000Mbps Fiber Media PHY Operating Mode

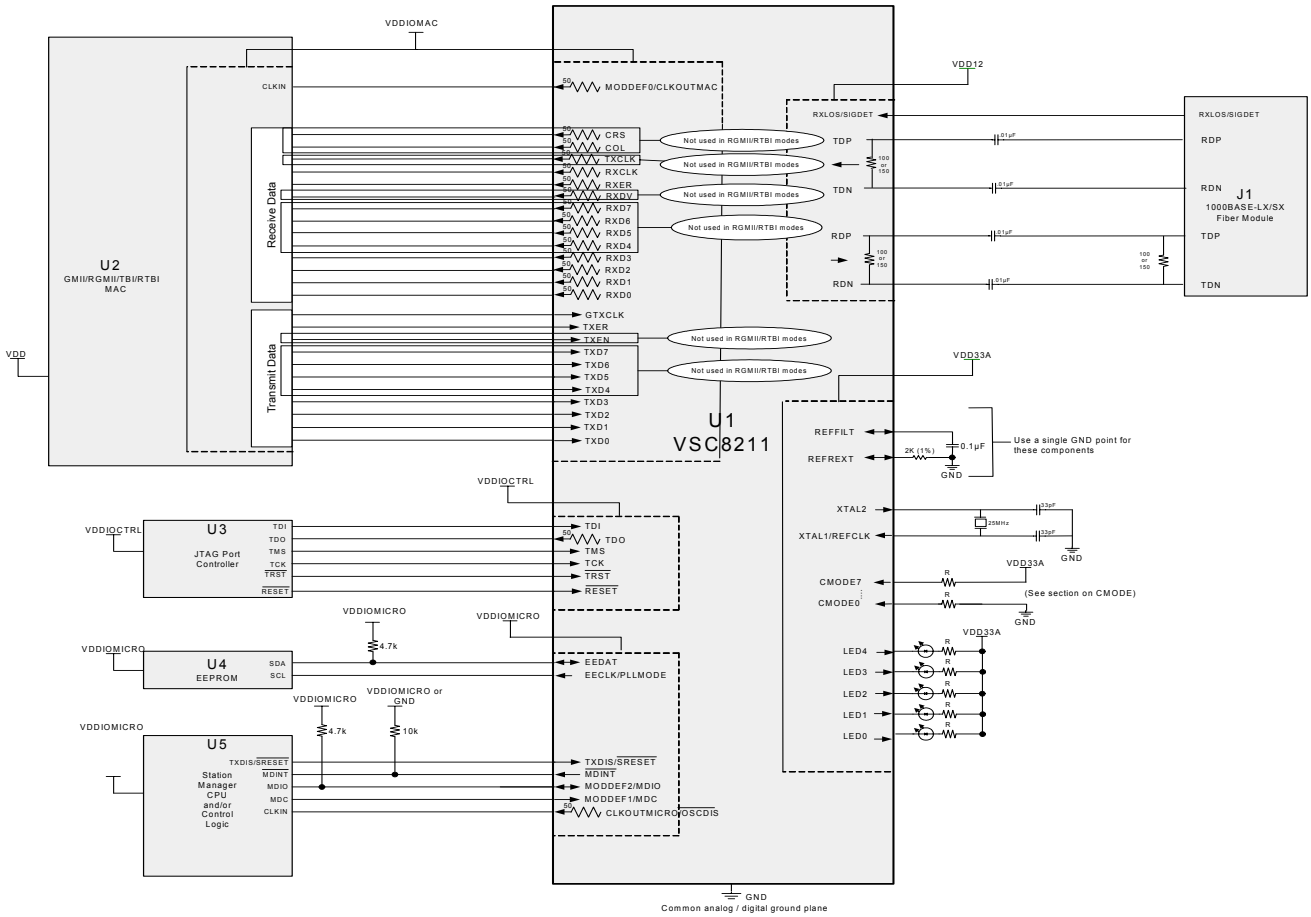


Figure 9. System Schematic – 'Parallel Data MAC to 1000Mbps Fiber Media' PHY Operating Mode

10.3 Parallel Data MAC to Copper/Fiber Auto Media Sense PHY Operating Mode

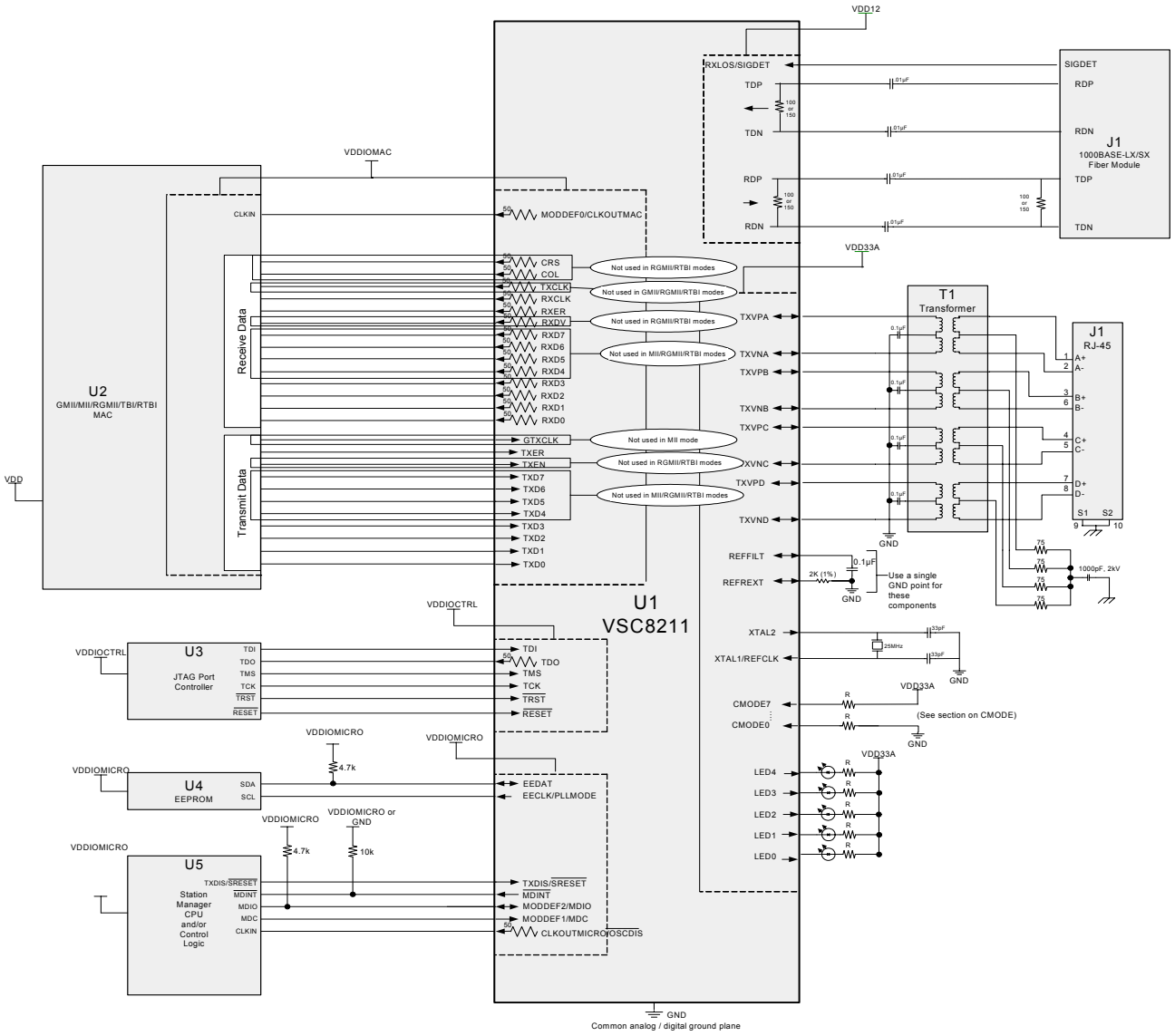


Figure 10. System Schematic – 'Parallel Data MAC to Copper/Fiber Auto Media Sense' PHY Operating Mode

10.4 SGMII/802.3z SerDes MAC to CAT5 Media PHY Operating Mode

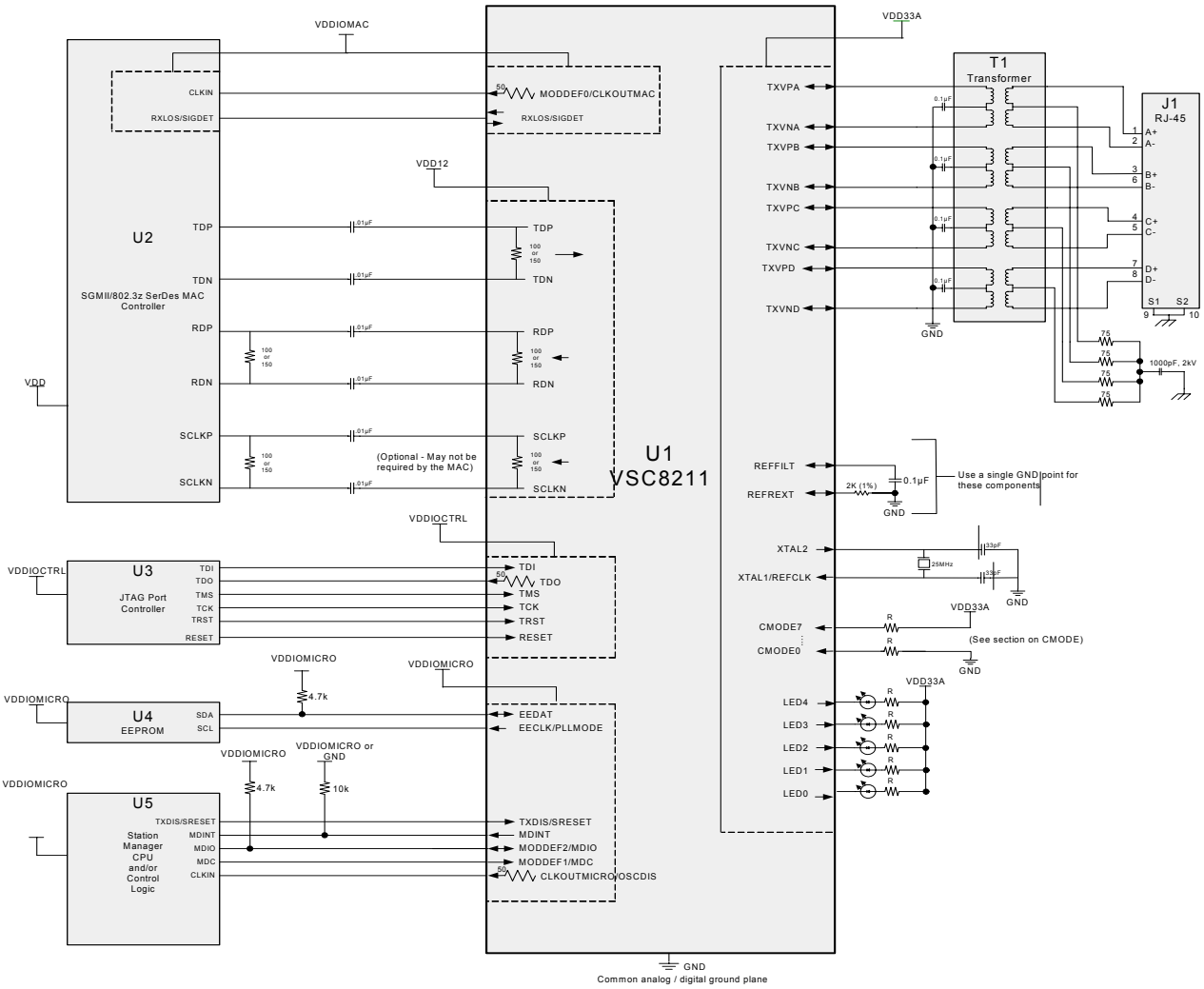


Figure 11. System Schematic – 'SGMII/802.3z SerDes MAC to CAT5 Media' PHY Operating Mode

10.5 SGMII/802.3z SerDes to 1000Mbps Fiber Media PHY Operating Mode

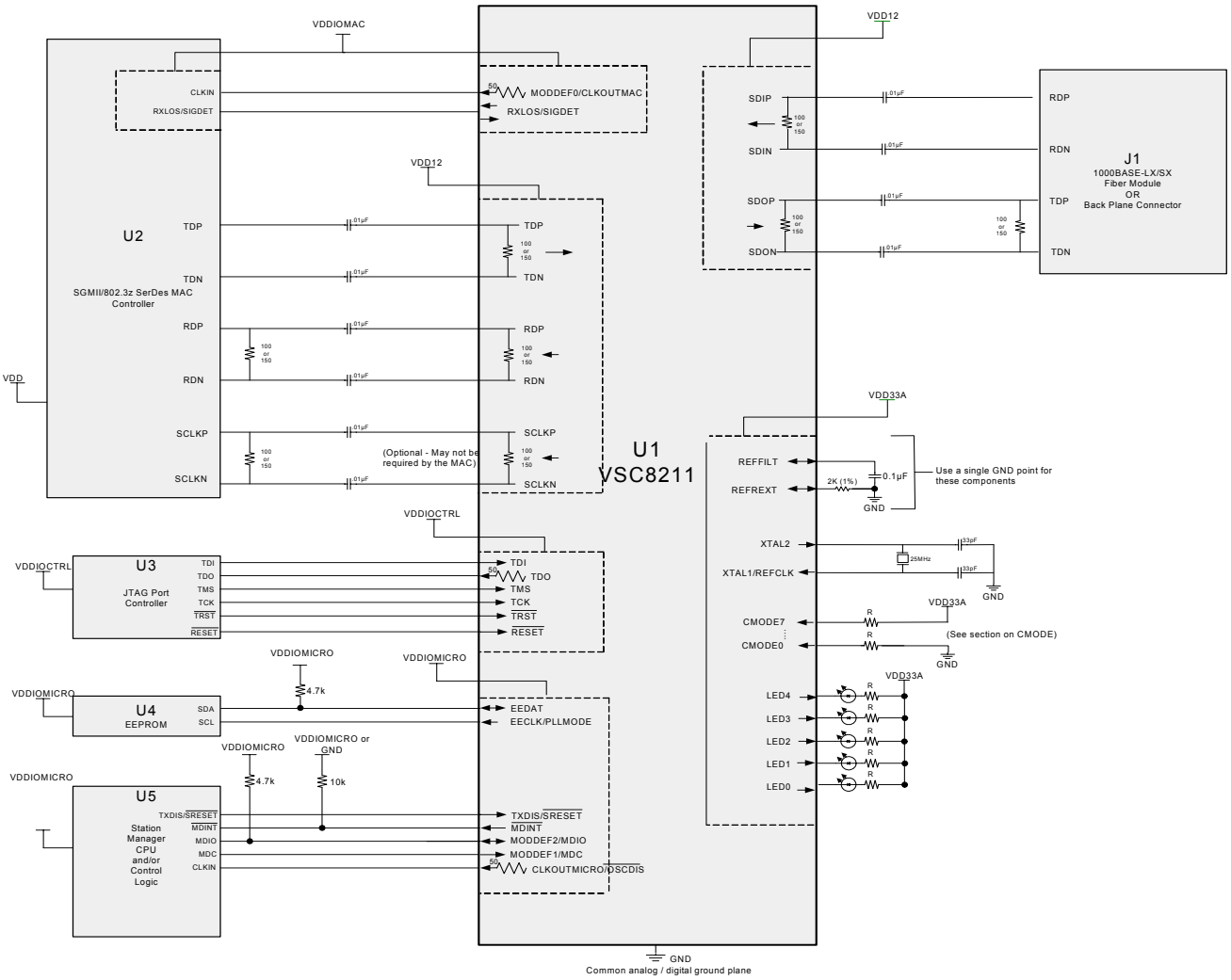


Figure 12. System Schematic – 'SGMII/802.3z SerDes to 1000Mbps Fiber Media' PHY Operating Mode

10.6 100Mbps Fiber Media Implementation

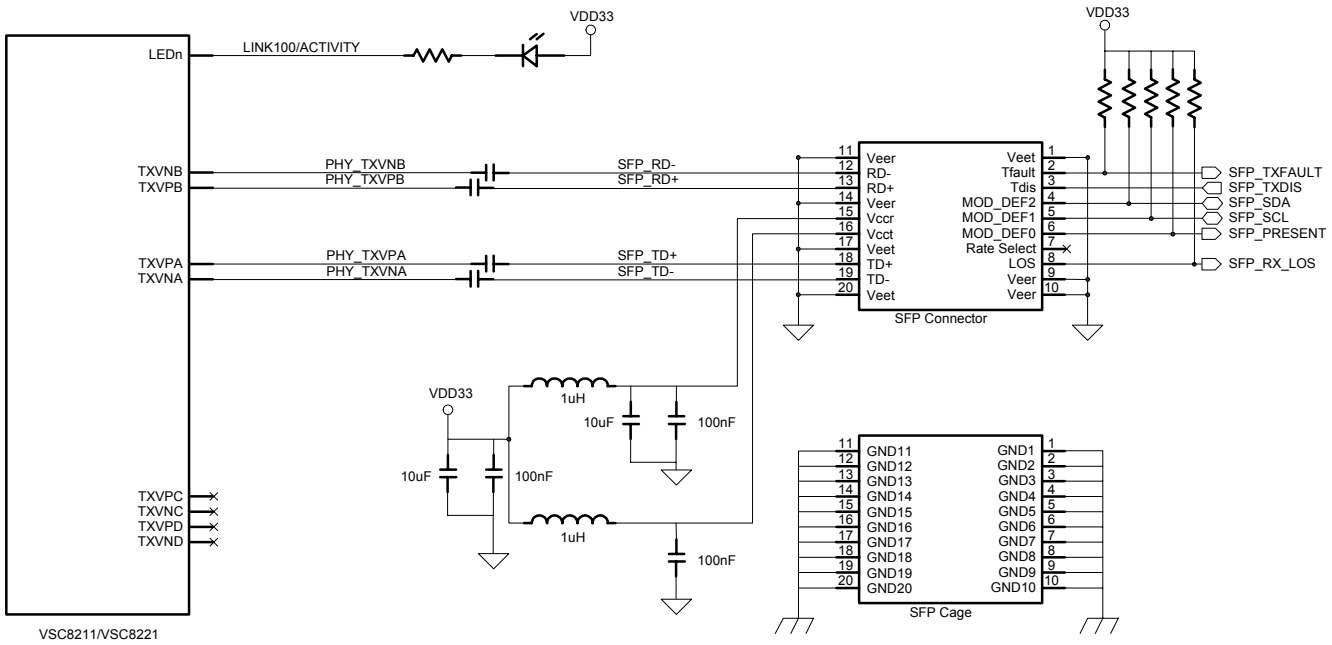


Figure 13. System Schematic – '100Mbps Fiber Media' Implementation

10.7 Serial MAC to Fiber/CAT5 Media PHY Operating Mode[1]

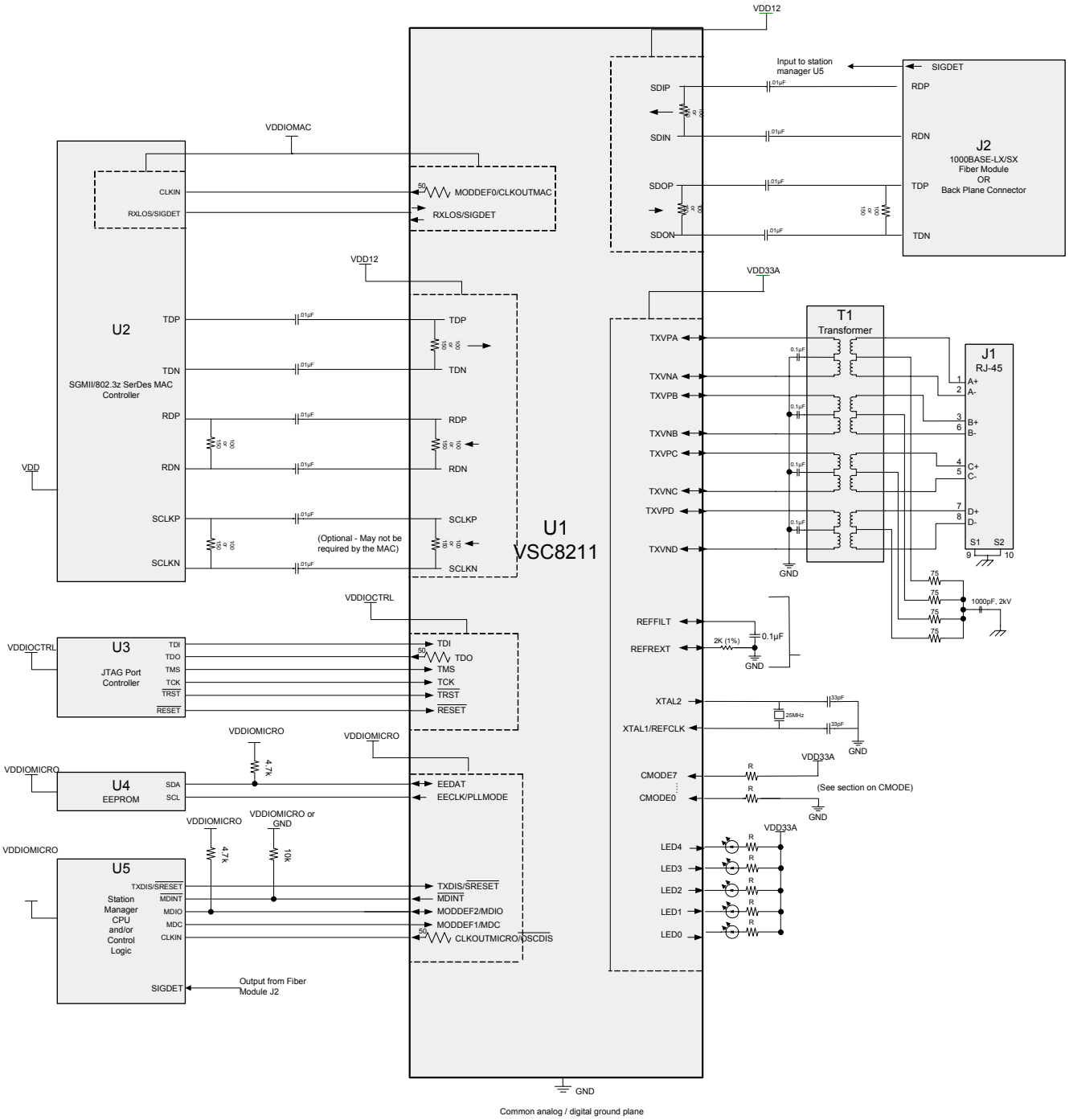


Figure 14. System Schematic - 'Serial MAC to Fiber/CAT5 Media' PHY Operating Mode

[1]The Transition from 'Serial MAC to CAT5' PHY Operating mode to 'Serial MAC to Fiber' PHY Operating mode and vice versa is managed by the 'Station Manager' by writing to PHY Register 23.15:12,2:1, based on the SIGDET input from the Fiber Optic connector.
Note that power supply sequencing is not needed to bring the device out of reset. Once the supplies are stable, the device reset can be de-asserted.

11 Twisted Pair Interface

The twisted pair interface on the VSC8211 is fully compliant with the IEEE802.3-2000 specification for CAT-5 media. All passive components necessary to connect the PHY to an external 1:1 transformer have been integrated into the VSC8211. The connection of the twisted pair interface is shown in the following figure:

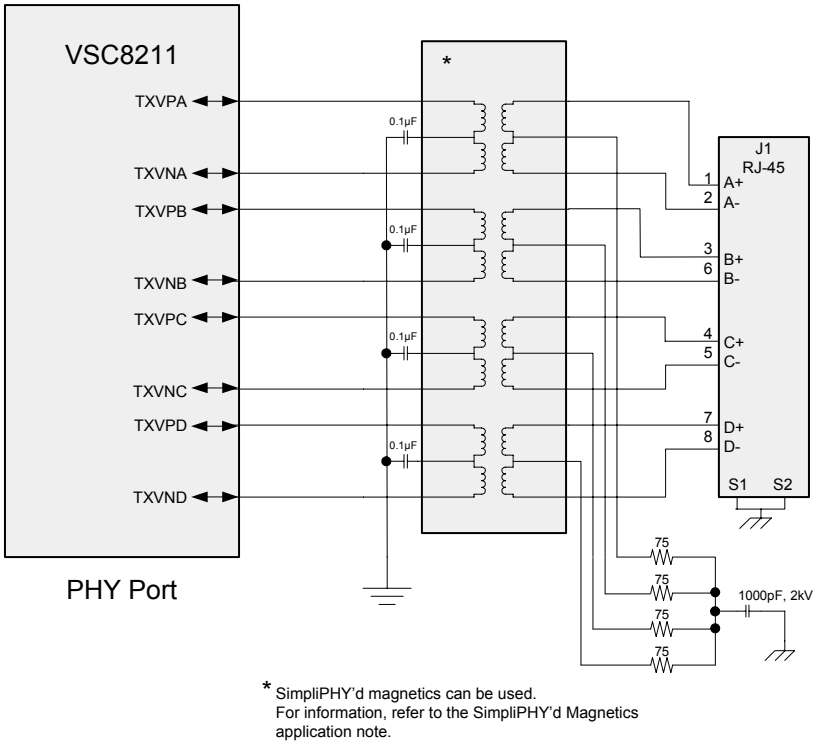


Figure 15. VSC8211 Twisted Pair Interface

Unlike other Gigabit PHYs, which do not integrate line terminations into the PHY, the VSC8211 device's twisted pair interface is compatible with a wide variety of standard magnetics and RJ-45 modules from common module vendors. Depending on the application (the number of ports, EMI performance requirements such as FCC Class A or B, the type and quality of the equipment shielding, and other EMI design practices in place, for example), the twisted pair interface may be used with standard (12- or 8-core) magnetics as well as SimpliPHY'd (4-core) magnetics modules available from many module vendors. In addition, this interface is also used to provide support for 100Mbps fiber module connection. For more information on the suitability of using SimpliPHY'd magnetics for a particular design, see the application note *SimpliPHY'd Magnetics and EMI Control*, available from the Vitesse website.

11.1 Twisted Pair Autonegotiation (IEEE802.3 Clause 28)

The VSC8211 supports twisted pair autonegotiation, as defined in IEEE 802.3-2002 clause 28. (However, autonegotiation is not defined by IEEE for the 100BASE-FX mode and is therefore not supported.) This process evaluates the advertised capabilities of the local PHY and its link partner to determine the best possible operating mode. In particular, autonegotiation can determine speed, duplex, and MASTER/SLAVE modes for 1000BASE-T. Autonegotiation also allows the local MAC to communicate with the Link Partner MAC (via optional "Next-Pages") to set attributes that may not be defined in the standard. If the link partner does not support autonegotiation, the VSC8211 will automatically use parallel-detect to select the appropriate link speed.

Clause 28 twisted-pair autonegotiation can be disabled by clearing bit MII Register bit 0.12 – Auto-Negotiation Enable. If autonegotiation is disabled, the operating speed and duplex mode of the VSC8211 is determined by the state of MII Register bits 0.13, 0.6 – Forced Speed Selection and MII Register bit 0.8 – Duplex Mode. For more information, see "Register 0 (00h) – Mode Control Register - Clause 28/37 View" on page 85.

11.2 Twisted Pair Auto MDI/MDI-X Function

For trouble-free configuration and management of Ethernet links, the VSC8211 includes robust Automatic Crossover Detection functionality for all three speeds on the twisted pair interface (10BASE-T, 100BASE-TX, and 1000BASE-T) – fully compliant with the IEEE standard. In addition, the VSC8211 detects and corrects polarity errors on all MDI pairs, beyond what is required by the standard. Both the Automatic MDI/MDI-X and Polarity Correction functions are enabled by default. However, complete user control of these two features is available using bits 5 and 4 of the Bypass Control register. For more information, see "Register 18 (12h) – Bypass Control Register" on page 103. Status bits for each of these functions are located in Register 28 (1Ch) – Auxiliary Control & Status Register.

The VSC8211's Automatic MDI/MDI-X algorithm will successfully detect, correct, and operate with any of the MDI wiring pair combinations listed in the following table:

Table 16. Accepted MDI Pair Connection Combinations

	RJ-45 Connections				Comments
	1,2	3,6	4,5	7,8	
MDI Pair Connection Combinations Accepted by VSC8211	A	B	C	D	Normal MDI mode Normal DTE/NIC mode No crossovers
	B	A	C	D	MDI-X mode Normal for switches & repeaters Crossover on A and B pairs only
	A	B	D	C	Normal MDI mode Normal for DTEs (NICs) No crossovers Pair swap on C and D pairs
	B	A	D	C	Normal MDI-X mode Normal switch/repeater mode Crossovers assumed Crossover on A and B pairs Pair swap on C and D pairs

11.3 Auto MDI/MDI-X in Forced 10/100 Link Speeds

The VSC8211 includes the ability to perform Auto MDI/MDI-X even when auto-negotiation is disabled (MII Register 0.12 = 0) and the link is forced into 10/100 link speeds. In order to enable this feature, additional MII register write settings are also needed in the following order:

To enable Auto MDI/MDI-X in forced 10/100 link speeds:

- Write MII Register 31 = 0x2A30
- Write MII Register 8 = 0x0212
- Write MII Register 31 = 0x52B5
- Write MII Register 2 = 0x0012
- Write MII Register 1 = 0x2803
- Write MII Register 0 = 0x87FA
- Write MII Register 31 = 0x2A30
- Write MII Register 8 = 0x0012
- Write MII Register 31 = 0x0000

To disable Auto MDI/MDI-X in forced 10/100 link speeds:

- Write MII Register 31 = 0x2A30

- Write MII Register 8 = 0x0212
- Write MII Register 31 = 0x52B5
- Write MII Register 2 = 0x0012
- Write MII Register 1 = 0x3003
- Write MII Register 0 = 0x87FA
- Write MII Register 31 = 0x2A30
- Write MII Register 8 = 0x0012
- Write MII Register 31 = 0x0000

11.4 Twisted Pair Link Speed Downshift

In addition to automatic crossover detection, the VSC8211 supports an automatic link speed “downshift” option for operation in cabling environments incompatible with 1000BASE-T. When this feature is enabled, the VSC8211 will automatically change its autonegotiation advertisement to 100BASE-TX after a set number of failed attempts at 1000BASE-T. This is especially useful in setting up networks using older cable installations which may include only pairs A and B and not pairs C and D. The link speed downshift feature is configured and monitored using Register 20E (14h) - Extended PHY Control Register #3.

11.5 100Mbps Fiber Support Over Copper Media Interface

The VSC8211 supports 100BASE-FX over its copper media interface by using pairs A and B, which provide TX and RX differential connections, respectively. If the fiber module does not have internal AC coupling capacitors, then they are required between the PHY and fiber module. The value should be 0.1µF.

The RXLOS/SIGDET signal is not used in this mode.

A separate 1000BASE-X fiber module may be connected to the PHY through the 1000BASE-X SerDes pins.

11.5.1 Register Settings

The PHY can be brought into the 100BASE-FX operation mode using the following configuring sequence:

1. Initialize the PHY into the specific MAC-to-copper operating mode for the MAC interface type required (register 23).
2. Disable Auto-Negotiation and force the 100BASE-T FDX mode (register 0).
3. Run the 100BASE-FX initialization script; for more information, see Section 33.4: "100BASE-FX Initialization Script".
4. Configure other settings, such as LEDs.

12 Transformerless Operation for PICMG 2.16 and 3.0 IP-based Backplanes

The twisted pair interface supports capacitively coupled links, such as those specified by the PICMG 2.16 and 3.0 specifications. With proper AC coupling, the typical category-5 magnetic isolation can be replaced with capacitors. For more information, see “Register 24 (18h) – PHY Control Register #2,” page 111, and the Vitesse application note “Transformerless Ethernet Concept and Applications”.

By enabling the PICMG Miser mode, power consumption can be reduced to approximately 500mW.

13 Dual Mode Serial Management Interface (SMI)

The Serial Management Interface provides access to the PHY registers for device configuration and Status Information. It also provides access to the EEPROM connected to the EEDAT and EECLK pins (EEPROM Interface) of the PHY. For details on EEPROM access through the SMI interface refer to Section 20: "EEPROM Interface".

The MODDEF1/MDC, MODDEF2/MDIO, and the $\overline{\text{MDINT}}$ pins comprise the SMI interface.

By writing to MII Register 21E.15 at startup (Refer to Section 19: "Hardware Configuration Using CMODE Pins" and Section 20: "EEPROM Interface" for details), the SMI of the PHY can be set to operate in one of the following two modes:

1. MSA
2. IEEE

13.1 PHY Register Access with SMI in MSA mode

In this mode, the PHY registers are accessed using the standard MSA compliant protocol. This protocol is generally used for reading and writing to Atmel's AT24 series compatible EEPROMs.

In this mode, the SMI pins function as follows:

Table 17. SMI Pin Descriptions - MSA Mode

Pin Name	Description
MODDEF1	Clock Input. Connect to the SCL pin of the AT24 series of EEPROMs.
MODDEF2	Bidirectional Data. Connect to the SDA pin of the AT24 series of EEPROMs. This pin should be pulled high on the board using a 4.7kΩ to 10kΩ pull-up resistor.
$\overline{\text{MDINT}}$	Interrupt Signal.

According to the protocol described in the MSA specification, the following conditions are defined:

- **Start [S]:** A high to low transition on the MODDEF2 pin when MODDEF1 is high.
- **Data [D]:** A transition on the MODDEF2 pin when MODDEF1 is low. A low to high transition is '1' and a high to low transition is '0'.
- **Stop [T]:** A low to high transition on the MODDEF2 pin when MODDEF1 is high.
- **Acknowledge (By Receiver) [A]:** A low driven by the PHY/Receiver after 8 Data states. The transition on MODDEF2 takes place when MODDEF1 is low. The host does not drive the MODDEF2 Data line in this condition.
- **Acknowledge (By Host) [H]:** A low driven by the host after 8 Data states. The transition on MODDEF2 takes place when MODDEF1 is low. The PHY/Receiver does not drive the MODDEF2 Data line in this condition.
- **No Acknowledge (By Host) [N]:** A high driven by the host after 8 Data states. The transition on MODDEF2 takes place when MODDEF1 is low. The PHY/Receiver does not drive the MODDEF2 Data line in this condition.

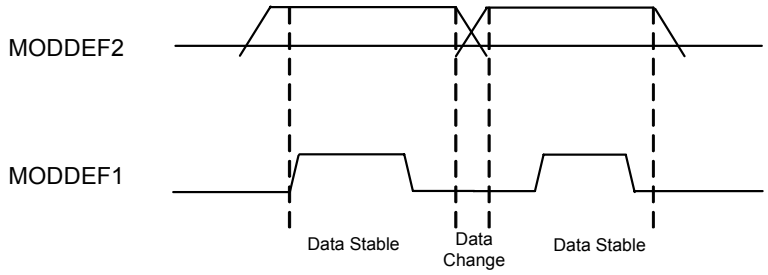


Figure 16. Data Validity

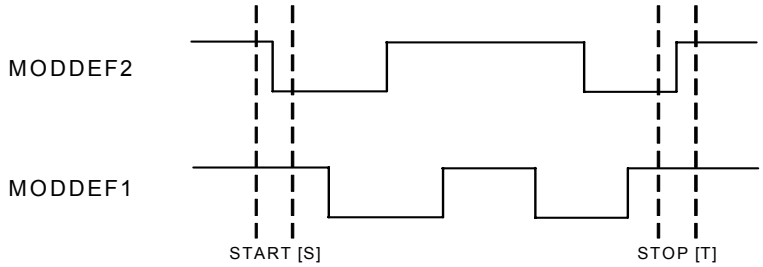


Figure 17. Start [S] and Stop [T] Definition

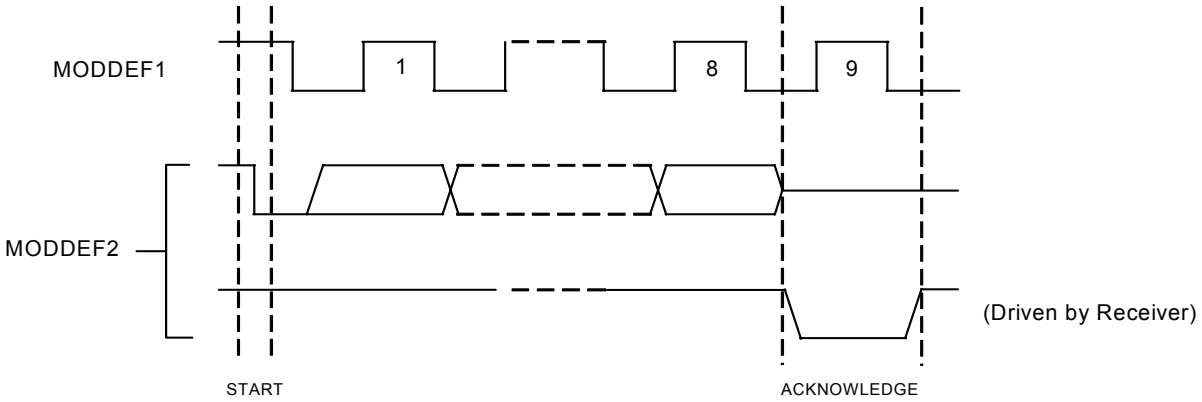


Figure 18. Acknowledge (By Receiver) [A]

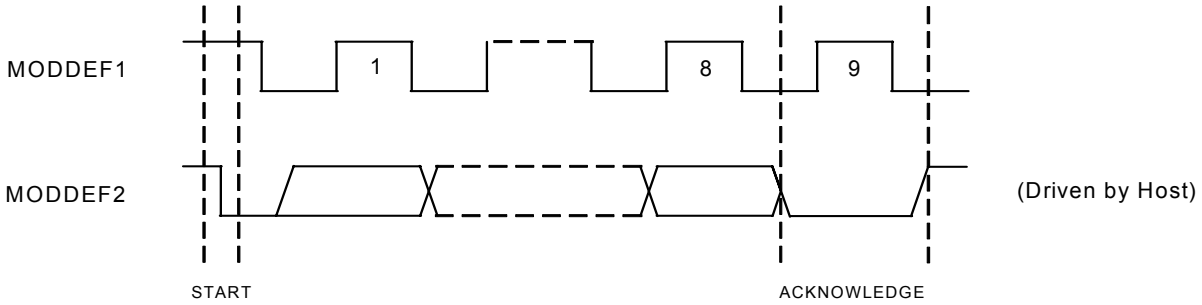


Figure 19. Acknowledge (By Host) [H]

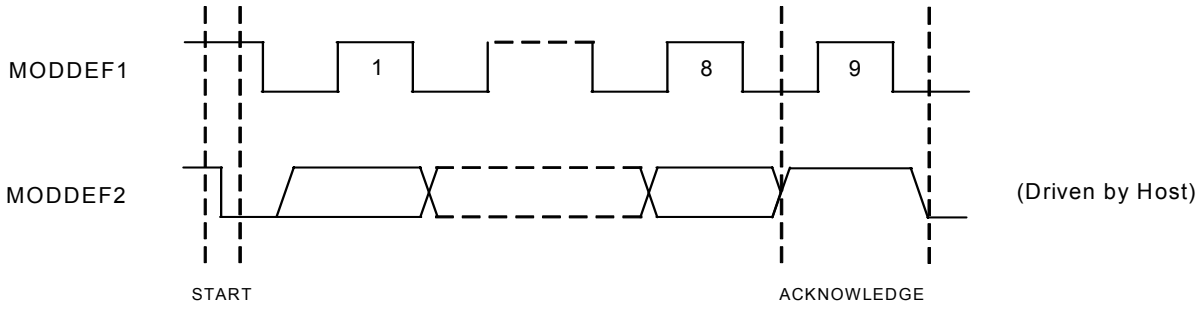


Figure 20. No Acknowledge (By Host) [N]

13.1.1 Write Operation - Random Write

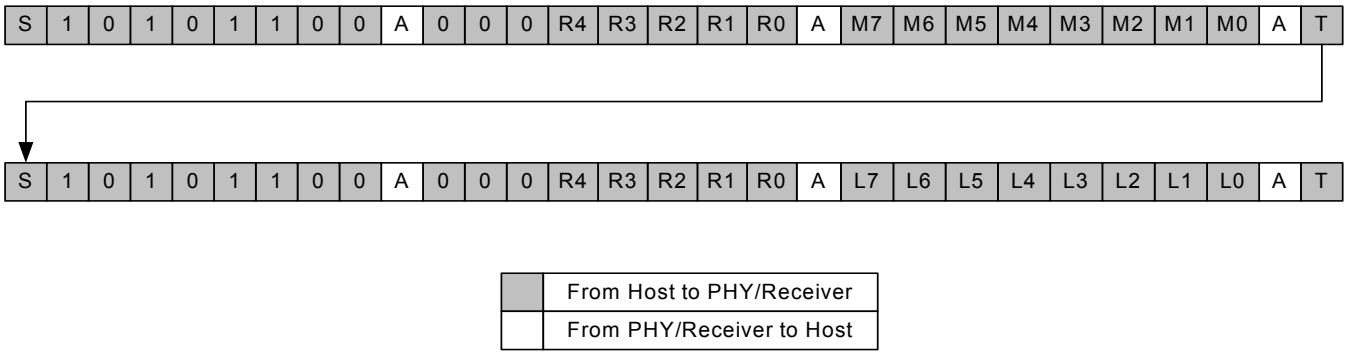


Figure 21. Random Write

- R4..R0 are the 5 bits of the Register address R.
- M7..M0 are bits of the Upper byte of the 16 bit Register data
- L7..L0 are bits of the Upper byte of the 16 bit Register data

The PHY register is written only after the host performs the lower data byte write operation.

13.1.2 Write Operation - Sequential Write

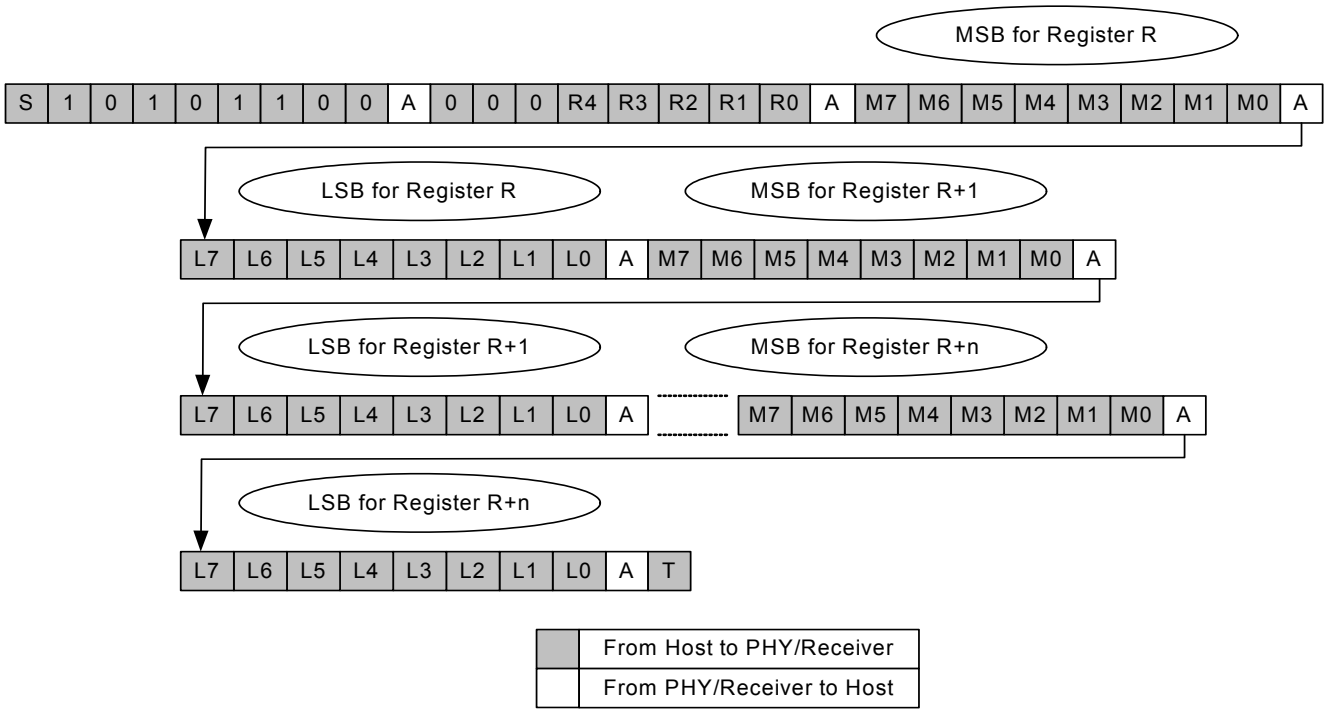


Figure 22. Sequential Write

- R4..R0 are the 5 bits of the Register address R.
- M7..M0 are bits of the Upper byte of the 16 bit Register data
- L7..L0 are bits of the Upper byte of the 16 bit Register data

The PHY register is written only after the host performs the lower data byte write operation.

13.1.3 Read Operation - Random Read

Figure 23. Random Read

- R4..R0 are the 5 bits of the Register address
- M7..M0 are bits of the Upper byte of the 16 bit Register data
- L7..L0 are bits of the Lower byte of the 16 bit Register data

13.1.4 Read Operation - Sequential Read

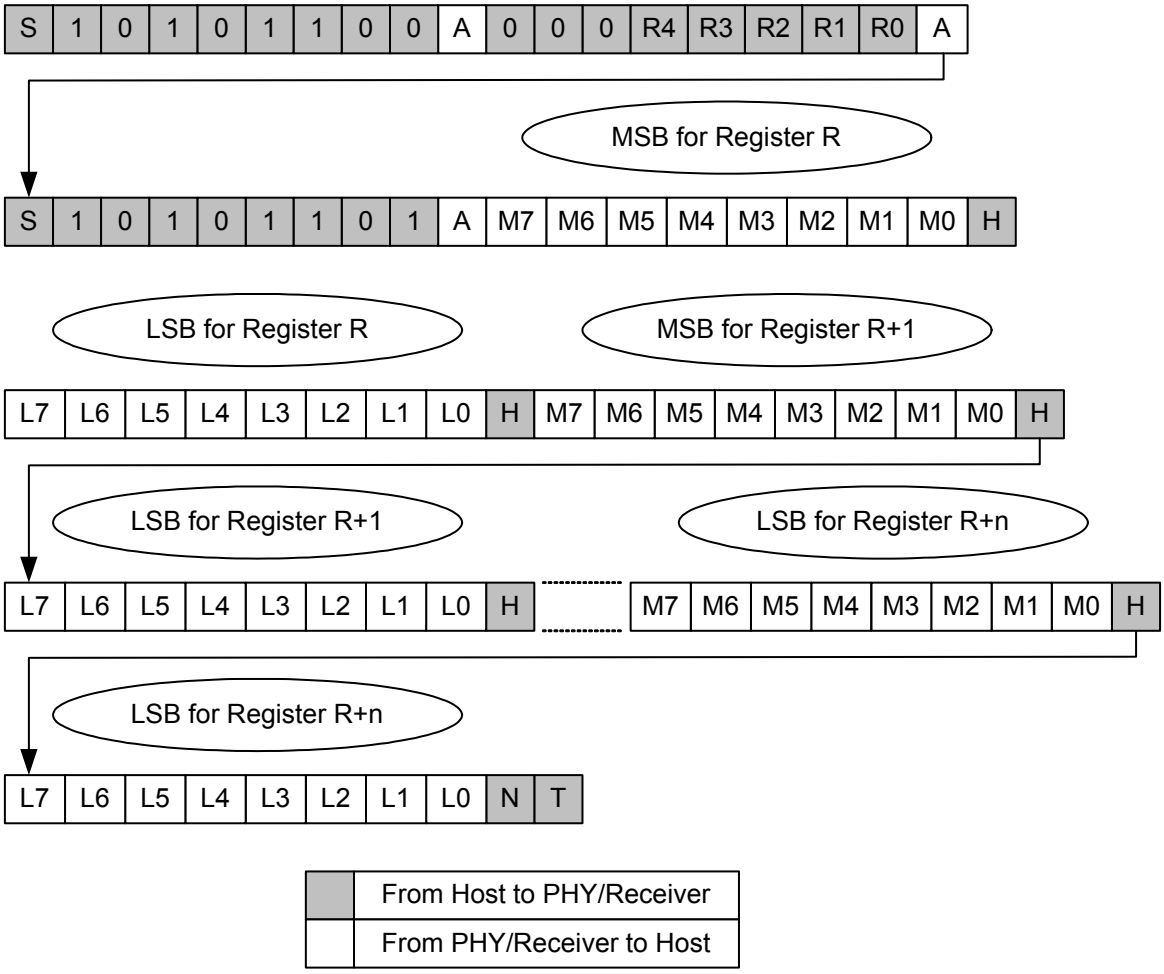


Figure 24. Sequential Read

- R4..R0 are the 5 bits of the Register address
- M7..M0 are bits of the Upper byte of the 16 bit Register data
- L7..L0 are bits of the Lower byte of the 16 bit Register data

13.2 PHY Register Access with SMI in IEEE Mode

In IEEE mode, the SMI is fully compliant with the IEEE 802.3-2000 MII Interface specifications.

In IEEE mode, the SMI pins function as follows:

Table 18. SMI Pin Descriptions - MSA Mode

Pin Name	Description
MDC	Clock Input, 0 – 12.5 Mhz.
MDIO	Bidirectional Data. This pin should be pulled high on the board using a 4.7kΩ to 10kΩ resistor.
$\overline{\text{MDINT}}$	Active Low or Active High open drain interrupt output.

As many as 32 PHYs (32 distinct PHY Addresses) can share a common IEEE SMI signal pair (MDC, MDIO).

Data is transferred over the IEEE SMI using 32-bit frames with an optional and arbitrary length preamble. The IEEE SMI frame format is described in the following table.

Table 19. SMI Frame Format

	Direction from VSC8211	Preamble	Start of Frame	Op Code	PHY Address	Register Address	Turn-Around	Data	Idle
# of bits		1+	2	2	5	5	2	16	?
Read	Output	Z's	ZZ	ZZ	Z's	Z's	Z0	data	Z's
	Input	1's	01	10	addr	addr	ZZ	Z's	Z's
Write	Output	Z's	ZZ	ZZ	Z's	Z's	ZZ	Z's	Z's
	Input	1's	01	01	addr	addr	10	data	Z's

- Idle: During idle, the MDIO node goes to a high-impedance state. This allows an external pull-up resistor to pull the MDIO node up to a logical “1” state. Since idle mode should not contain any transitions on MDIO, the number of bits is undefined during idle.
- Preamble: For the VSC8211, the preamble is optional. By default, preambles are not expected or required. The preamble is a string of “1”s. If it exists, the preamble must be at least one bit, but otherwise my be arbitrarily long. See MII Register 1.6 for more information.
- Start of frame: A “01” pattern indicates the start of frame. If these bits are anything other than “01”, all following bits are ignored until the next “preamble:0” pattern is detected.
- Operation code: A “10” pattern indicates a read. A “01” pattern indicates a write. If these bits are anything other than “01” or “10”, all following bits are ignored until the next “preamble:0” pattern is detected.
- PHY address: The next five bits are the PHY address. The PHY responds to a message frame only when the received PHY address matches its physical address. The PHY's address is indicated by the CMODE1[2] and CMODE0[3:0] bits.
- Register address: The next five bits are the register address.
- Turn-around: The next two bits are “turn-around” (TA) bits. They are used to avoid contention when a read operation is performed on the MDIO. During read operations, the VSC8211 will drive the second TA bit, which is a logical “0”.
- Data: The next sixteen bits are data bits. When data is being read from the PHY, data is valid at the output of the PHY from one rising edge of MDC to the next rising edge of MDC. When data is being written to the PHY, data must be valid around the rising edge of MDC.
- Idle: The sequence is repeated.

The following two figures diagram IEEE SMI read and IEEE SMI write operations.

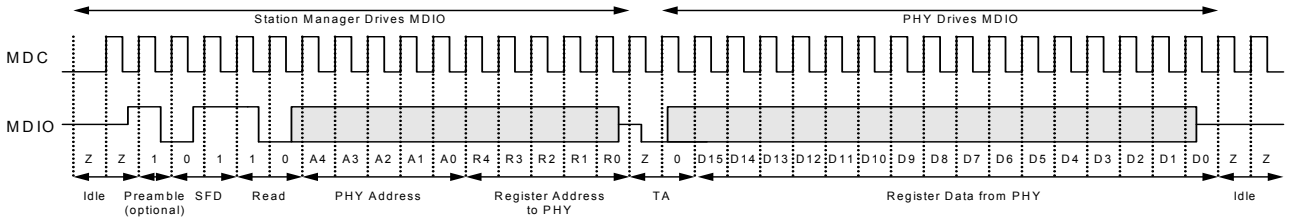


Figure 25. MDIO Read Frame

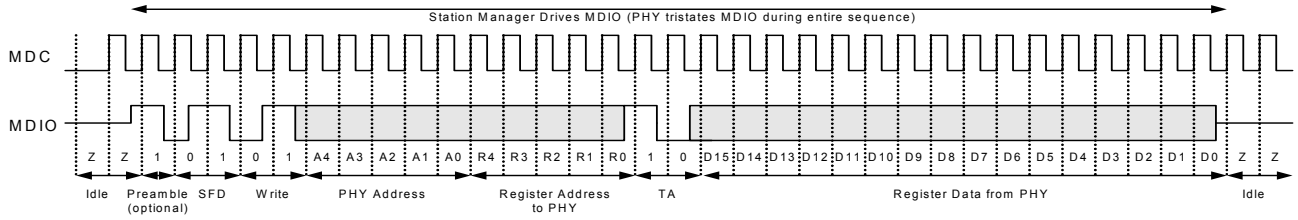


Figure 26. MDIO Write Frame

13.3 SMI Interrupt

The SMI includes an output signal $\overline{\text{MDINT}}$ for signaling the Station Manager when certain events occur in the PHY. The $\overline{\text{MDINT}}$ pin can be configured for active-low or active-high operation by tying the pin to either a pull-up resistor to VDDIOMICRO or to a pull-down resistor to GND.

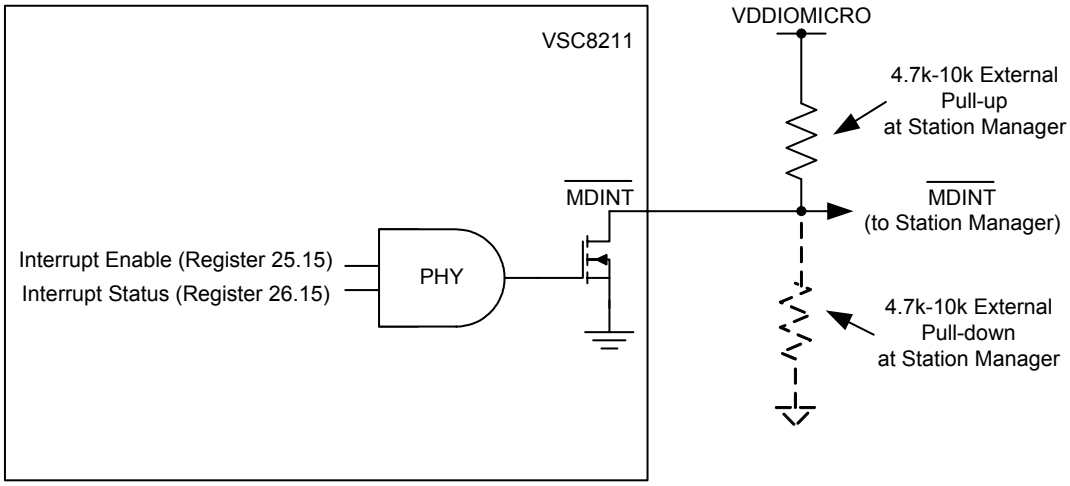


Figure 27. Logical Representation of $\overline{\text{MDINT}}$ Pin

14 LED Interface

The PHY has five dedicated LED[4:0] pins to drive 5 LEDs directly. For power savings, all LED outputs can be configured to pulse at 5kHz with a 20% duty cycle. All LED outputs are active-low and driven with 3.3V from the VDD33A power supply when deasserted.

Due to the fact that the 100BASE-FX mode uses 100BASE-T resources, its indications are those of the 100BASE-T mode.

Four different functions have been assigned to each LED pin. Selection is done using either the CMODE hardware configuration (see Section 19: "Hardware Configuration Using CMODE Pins") or the settings in Register 27 (1Bh) – LED Control Register, page 117. The functions are assigned according to the following table:

Table 20. LED Function Assignments

LED Configuration Bits	Value	LED Function Selection
LED Pin 4 Config [1:0]	11	TX
	10	Fault
	01	Activity
	00	Duplex/Collision
LED Pin 3 Config [1:0]	11	RX
	10	Fiber
	01	Duplex/Collision
	00	Link/Activity
LED Pin 2 Config [1:0]	11	TX
	10	Link/Activity
	01	Duplex/Collision
	00	Link10/Activity
LED Pin 1 Config [1:0]	11	Link100/1000/Activity
	10	Link/Activity
	01	Link10/100/Activity
	00	Link100/Activity
LED Pin 0 Config [1:0]	11	RX
	10	Fault
	01	Link/Act (with serial output on LED pins 1 and 2)
	00	Link1000/Activity

LED functions are summarized in the following table.

Table 21. Parallel LED Functions

Function Name	State	Description
Link1000/Activity[1]	1	No link in 1000BASE-T or 1000BASE-X
	0	Valid 1000BASE-T link or 1000BASE-X link
	Pulse-stretch/Blink[2]	(optional) Valid 1000BASE-T link and activity present

Table 21. Parallel LED Functions *(continued)*

Function Name	State	Description
Link100/Activity[1]	1	No link in 100BASE-Tx
	0	Valid 100BASE-Tx link
	Pulse-stretch/Blink[2]	(optional) Valid 100BASE-Tx link and activity present
Link10/Activity[1]	1	No link in 10BASE-T
	0	Valid 10BASE-T link
	Pulse-stretch/Blink[2]	(optional) Valid 10BASE-T link and activity present
Link10/100/ Activity[1]	1	No link in 10BASE-T or 100BASE-Tx
	0	Valid 10BASE-T link or valid 100BASE-Tx link
	Pulse-stretch/Blink[2]	(optional) Valid 10BASE-T link or valid 100BASE-Tx link and activity present
Link100/1000/ Activity[1]	1	No link in 100BASE-Tx or 1000BASE-T
	0	Valid 100BASE-Tx link or valid 1000BASE-T link
	Pulse-stretch/Blink[2]	(optional) Valid 100BASE-Tx link or valid 1000BASE-T link and activity present
Link/Act[1]	1	No link in any speed
	0	Valid link in any speed
	Pulse-stretch/Blink[2]	Valid link in any speed and activity present
Collision	1	No collisions detected
	Pulse-stretch/blink[2]	Collisions detected
Activity	1	No activity
	Pulse-stretch/blink[2]	Activity present
Fiber	1	No valid 1000BASE-X link established
	0	Fiber media detected on SerDes interface and valid 1000BASE-X link established
Fault	1	No IEEE Clause 37/28 autonegotiation fault
	0	IEEE Clause 37/28 autonegotiation fault
Serial	**	See serial interface specification
Duplex/Collision[3]	1	Link established in half-duplex mode, or no link established
	0	Link established in full-duplex mode
	Pulse-stretch/Blink[2]	(optional) Link established in half duplex mode and collisions present
Rx	1	No activity on Rx side
	Pulse-stretch/blink[2]	Activity present on Rx side
Tx	1	No activity on Tx side
	Pulse-stretch/blink[2]	Activity present on Tx side

[1] By default the ‘Link’ functions are combined with ‘Activity’. To use the LED as a dedicated ‘Link’, LED MII register bit 27.1 must be set.
[2] Function can either blink or be pulse-stretched when active. See Table 22 below.
[3] By default the ‘Duplex’ function is combined with ‘Collision’. To use the LED as a dedicated ‘Duplex’, LED MII register bit 27.0 must be set.

In addition to function selection, several options are available for the LED outputs through the use of MII register 27.5:0. These are summarized below:

Table 22. LED Output Options

MII Reg Bits	LED Option Bits	Value	LED Function Selection
5:4	LED Blink/Pulse-Stretch Rate	11	2.5Hz blink rate/ 400 ms pulse-stretch
		10	20Hz blink rate/ 50ms pulse-stretch
		01	10Hz blink rate/ 100ms pulse-stretch
		00	5Hz blink rate/ 200ms pulse-stretch
3	LED pulse-stretch/blink	1	Collision, Activity, Rx and Tx LED outputs will be pulse-stretched when active
		0	Collision, Activity, Rx and Tx LED outputs will blink when active
2	LED Pulsing Enable	1	When active, LED outputs will be pulsed at 5KHz, 20% duty cycle for power savings
		0	When active, LED outputs will remain at a static low
1	LED combine LINK with ACT	1	Link LEDs indicate link status only
		0	Link LEDs will blink or flash when activity is present. Blink/flash behavior is selected by Pulse-Stretch Enable bit.
0	LED combine COL with DUP	1	Duplex LED indicates duplex status only
		0	Duplex LED will blink or flash when collision is present. Blink/flash behavior is selected by Pulse-Stretch Enable bit.

14.1 Serial LED Output

A serial output option is available which allows access to all LED signals through two pins. This option is selected by setting LED Pin 0 configuration bits to 01 on the PHY. In this mode, LED pins 1 and 2 function as serial data and clock. LED function outputs for the PHY are clocked out on the rising edge of data clock. The clock rate is approximately 1MHz, with a 37 clock cycle preamble.

The serial bitstream outputs each LED signal as described by the numbered list below.The individual signals shall be clocked out in the following order:

1. Link1000/Act
2. Link/Act
3. Link100/Act
4. Act
5. Link10/Act
6. Dup/Col
7. Tx
8. Col
9. Rx
10. Fault
11. Fiber/Copper

15 Test Mode Interface (JTAG)

The PHY supports the Test Access Port and Boundary Scan Architecture IEEE 1149.1 standards. The device includes an IEEE 1149.1 compliant test interface, often referred to as a “JTAG TAP Interface”. IEEE 1149.1 defined test logic provides the following standardized test methodologies:

- Testing the interconnections between integrated circuits once they have been assembled onto a printed circuit board or other substrate.
- Testing the integrated circuit itself during IC and systems manufacture.
- Observing or modifying circuit activity during the component’s normal operation.

The JTAG Test interface logic on the PHY, accessed through a Test Access Port (TAP) interface, consists of a boundary-scan register and other logic control blocks. The TAP controller includes all IEEE-required signals (TMS, TCK, TDI, and TDO), in addition to the optional asynchronous reset signal $\overline{\text{TRST}}$.

The following figure diagrams the TAP and Boundary Scan Architecture.

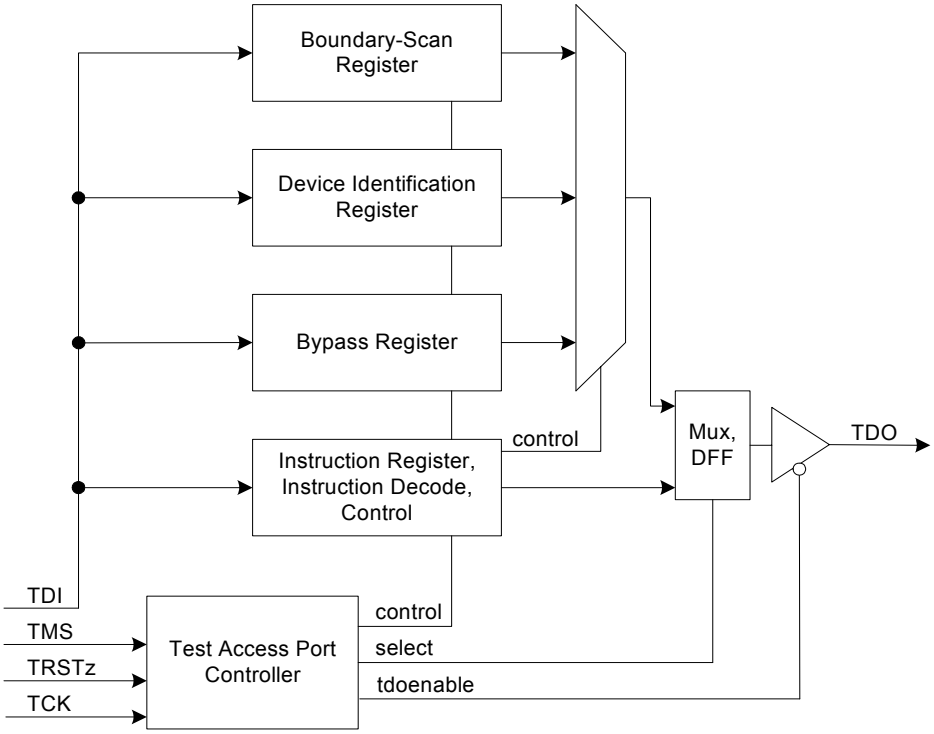


Figure 28. Test Access Port and Boundary Scan Architecture

The PHY also includes the optional Device Identification Register, shown in the following table, which allows the manufacturer, part number, and version number of the device to be determined through the TAP Controller.

See Chapter 11 of the IEEE 1149.1-1990 specifications for more details. Also, note that some of the information in the identification register is duplicated in the IEEE-specified bit fields in MII Register 3 (PHY Identifier Register #2).

Table 23. JTAG Device Identification Register Description

Description	Device Version Number (or Revision Code)	Part Number (or Model Number)	Vitesse's Manufacturer Identity	LSB
Bit Field	31 - 28	27 - 12	11 - 1	0
Binary Value	0001	1000 0010 0001 0001	001 1001 1000	1

15.1 Supported Instructions and Instruction Codes

After a TAP reset, the Device Identification Register is serially connected between TDI and TDO by default. The TAP Instruction Register is loaded either from a shift register (when a new instruction is shifted in), or, if there is no new instruction in the shift register, a hard-wired default value of 0110 (IDCODE) is loaded. Using this method, there is always a valid code in the instruction register, and the problem of toggling instruction bits during a shift is avoided. Unused codes are mapped to the BYPASS instruction.

The VSC8211 supports the instruction codes listed in the following table and described below.

Table 24. JTAG Interface Instruction Codes

Instruction	Code	Selected Register	Register Width	Specification
EXTEST	0000	Boundary-Scan Register	78	Mandatory IEEE 1149.1
SAMPLE/PRELOAD	0001	Boundary-Scan Register	78	Mandatory IEEE 1149.1
IDCODE	0110	Device Identification Register	32	Optional IEEE 1149.1
CLAMP	0010	Bypass Register	1	Optional IEEE 1149.1
HIGHZ	0011	Bypass Register	1	Optional IEEE 1149.1
BYPASS	0111	Bypass Register	1	Mandatory IEEE 1149.1
Reserved	0100, 1000, 1001, 1010, 1011, 1100, 1101, 1110, 1111			

EXTEST
The mandatory EXTEST instruction allows testing of off-chip circuitry and board-level interconnections by sampling input pins and loading data onto output pins. Outputs are driven by the contents of the boundary-scan cells, which have to be updated with valid values (with the PRELOAD instruction) prior to the EXTEST instruction.[1]

SAMPLE/PRELOAD
The mandatory SAMPLE/PRELOAD instruction allows a snapshot of inputs and outputs during normal system operation to be

[1]Following the use of this instruction, the on-chip system logic may be in an indeterminate state that will persist until a system reset is applied. Therefore, the on-chip system logic may need to be reset on return to normal (i.e., non-test) operation.

taken and examined. It also allows data values to be loaded into the boundary-scan cells prior to the selection of other boundary-scan test instructions.

IDCODE
The optional IDCODE instruction provides the version number (bits 31:28), and Vitesse's manufacturer identity (bits11:1), which can be serially read from the PHY. See "Register 3 (03h) – PHY Identifier Register #2 - Clause 28/37 View" on page 88 for the PHY-specific values for this instruction.

CLAMP
The optional CLAMP instruction allows the state of the signals driven from the component pins to be determined from the Boundary-Scan Register while the Bypass Register is selected as the serial path between TDI and TDO. While the CLAMP instruction is selected, the signals driven from the component pins will not change.[1]

HIGHZ
The optional HIGHZ instruction places the component in a state in which *all* of its system logic outputs are placed in a high impedance state. In this state, an in-circuit test system may drive signals onto the connections normally driven by a component output without incurring a risk of damage to the component. This makes it possible to use a board where not all of the components are compatible with the IEEE 1149.1 standard.[1]

BYPASS
The Bypass Register contains a single shift-register stage and is used to provide a minimum-length serial path (one TCK clock period) between TDI and TDO to bypass the device when no test operation is required.

15.2 Boundary-Scan Register Cell Order

All inputs and outputs are observed in the Boundary-Scan Register cells. All outputs are additionally driven by the contents of Boundary-Scan Register cells. Bidirectional pins have all three related Boundary-Scan Register cells: the input, the output, and the control. The full boundary scan cell order is available from Vitesse Semiconductor in *.BSD file format.

[1]Following the use of this instruction, the on-chip system logic may be in an indeterminate state that will persist until a system reset is applied. Therefore, the on-chip system logic may need to be reset on return to normal (i.e., non-test) operation.

16 Enhanced ActiPHY Power Management

In addition to the IEEE-specified power-down control bit (MII Register 0.11), the VSC8211 implements an Enhanced ActiPHY™ power management mode. This mode enables support for power-sensitive applications such as laptop computers with Wake-on-LAN™ capability. It utilizes a signal-detect function that monitors the media interface for the presence of a link to determine when to automatically power-down the PHY. The Station Manager is in control of this mode. The PHY then 'wakes up' at a programmable interval and attempts to 'wake-up' the link partner PHY by sending either a fast link pulse (FLP) over copper media or a Clause 37 restart signal over optical media.

The Enhanced ActiPHY™ power management mode can be set at startup (Refer to Section 19: "Hardware Configuration Using CMODE Pins" and Section 20: "EEPROM Interface" for details) or at any time during normal operation by writing to MII Register 28.6.

16.1 Operation in Enhanced ActiPHY Mode

There are three PHY operating states when Enhanced ActiPHY™ mode is enabled:

- Low power state
- LP Wake up state
- Normal operating state (link up state)

The PHY switches between the low power state and LP wake up state at a programmable rate (sleep timer) until signal energy has been detected on the media interface pins. When signal energy is detected, the PHY enters the normal operating state. When the PHY is in the normal operating state and link is lost, the PHY returns to the low power state after the link status time-out timer has expired. After reset, the PHY enters the low power state.

When autonegotiation is enabled in the PHY, the ActiPHY™ state machine will operate as described above. If autonegotiation is disabled and the link forced to 10BT or 100BTX modes while the PHY is in the low power state, the PHY continues to transition between the low power and LP Wake up states until signal energy is detected on the media pins. At that time, the PHY transitions to the normal operating state and stays in that state even when the link is dropped. If autonegotiation is disabled while the PHY is in the normal operation state, the PHY stays in that state when the link is dropped and does not transition back to the low power state.

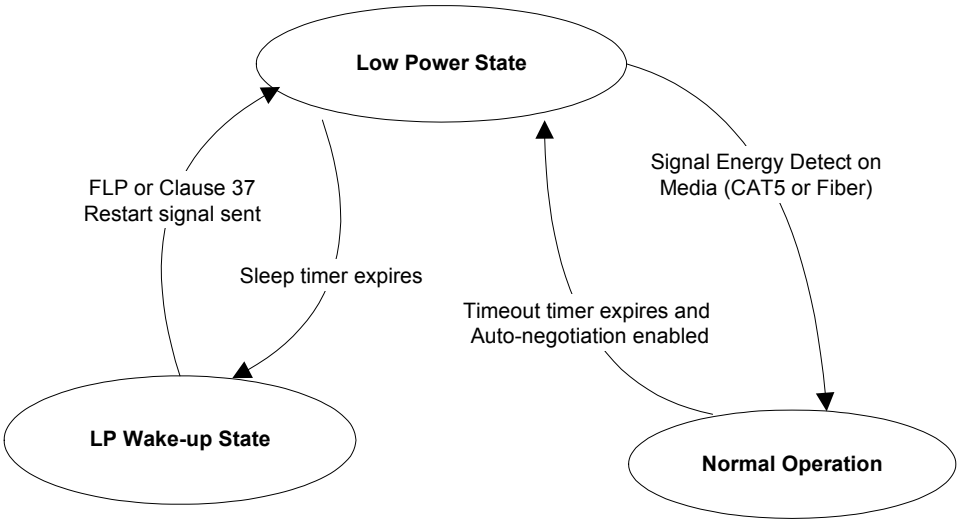


Figure 29. Enhanced ActiPHY State Diagram

16.2 Low power state

In the low power state, all major digital blocks are powered down. However the following functionality is provided:

- SMI interface (MDC/MODDEF1, MDIO/MODDEF2, $\overline{\text{MDINT}}$)
- CLKOUTMAC and CLKOUTMICRO

In this state, the PHY monitors the media interface pins for signal energy. The PHY comes out of low power state and transitions to the Normal operating state when signal energy is detected on the media. This happens when the PHY is connected to one of the following:

- Auto-negotiation capable link partner
- Auto-negotiation incapable (blind/forced) 100BTX only link partner
- Auto-negotiation incapable (blind/forced) 10BT only link partner
- Auto-negotiation capable optical link partner over fiber
- Auto-negotiation incapable (blind/forced) 1000BASE-X optical link partner over fiber
- Another PHY in Enhanced ActiPHY LP Wake Up state

In the absence of signal energy on the media pins, the PHY will transition from the low power state to the LP Wake up state periodically based on the programmable sleep timer. Two register bits (MII Register bits 28.1:0) are provided to program the value of the sleep timer. The sleep timer can be programmed to 2'b00 (1sec), 2'b01 (2sec), 2'b10 (3sec) or 2'b11 (4sec). The default value is 2 seconds. The actual sleep time duration is randomized by -80ms to +60ms to avoid two PHYs in Enhanced ActiPHY mode from entering a lock-up state.

16.3 LP Wake up state

In this state, the PHY attempts to wake up the link partner. One complete FLP (Fast Link Pulse) is sent on both pairs A and B of the CAT5 media. For the optical Media, a base page of all zeros (Clause 37 restart signal) is sent for 30ms.

In this state the following functionality is provided-

- SMI interface (MDC/MODDEF1, MDIO/MODDEF2, $\overline{\text{MDINT}}$)
- CLKOUTMAC and CLKOUTMICRO

After sending signal energy on the relevant media, the PHY returns to the Low power state.

16.4 Normal operating state

In this state, the PHY establishes a link with a link partner. When the media is unplugged or the link partner is powered down, the PHY waits for the duration programmed through a link status time-out timer and then enters the low power state. The Link Status Time-out timer can be programmed to 2'b00 (1sec), 2'b01 (2sec), 2'b10 (3sec), or 2'b11 (4sec). The default value for this timer is 2 seconds.

17 Ethernet In-line Powered Device Support

17.1 Cisco In-Line Powered Device Detection

This feature is used for detecting in-line powered devices in Ethernet network applications. The VSC8211's in-line powered device detection mode can be part of a system that allows for IP-phone and other devices to receive power from an Ethernet cable, similar to office digital phones receiving power from a PBX (Private Branch Exchange) office switch via the phone cable. This can eliminate the need for an IP-Phone to have an external power supply, since the Ethernet cable provides power. It also enables the in-line powered device to remain active during a power outage (assuming the Ethernet switch is connected to an uninterrupted power supply, battery, back-up power generator, etc.). This mode is disabled by default and must be enabled in order to perform in-line powered device detection. Please refer to additional information at http://www.cisco.com/en/US/products/hw/phones/ps379/products_tech_note09186a00801189b5.shtml for additional information.

17.2 In-Line Power Ethernet Switch Diagram

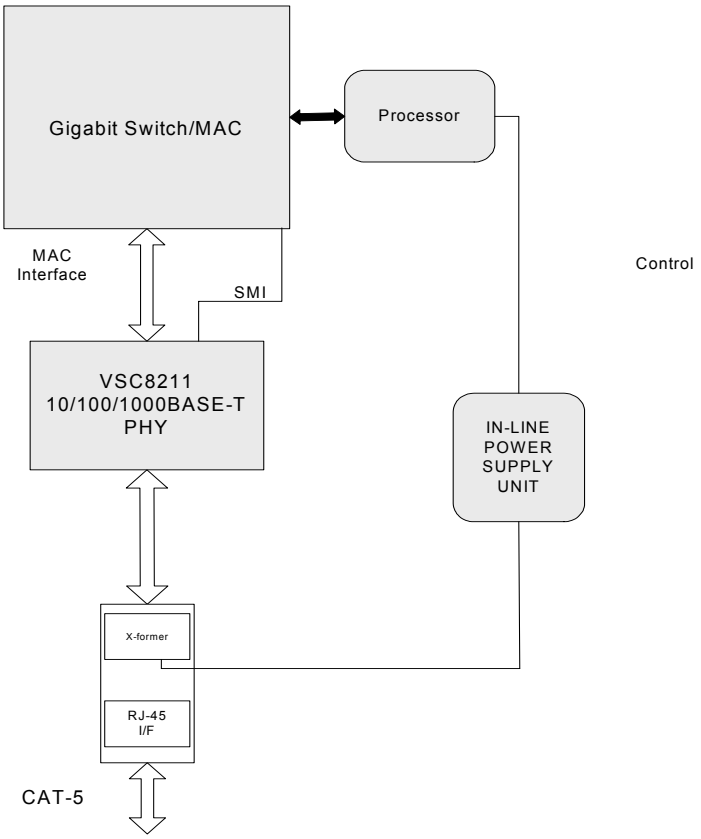


Figure 30. In-line Powered Ethernet Switch Diagram

17.3 In-Line Powered Device Detection (Cisco Method)

This section describes the flow process an Ethernet switch must perform in order to process in-line power requests made by a link partner (LP) capable of receiving in-line power.

1. The in-line powered device detection mode is enabled by setting MII Register bit 23E.10 = 1 and ensuring that the Auto-Negotiation Enable Bit is set (MII Register 0.12 = 1). An interrupt can also be asserted on the $\overline{\text{MDINT}}$ pin when in-line power is needed. This is set by MII Register 25.9 = 1 and ensuring MII Register 25.15 = 1 in order to enable the MDINT pin.
2. The PHY will then start sending a special Fast Link Pulse (FLP) signal to the LP. MII Register 23E.9:8 will equal 00 during the search for devices needing in-line power.

3. The PHY monitors for the special FLP signal looped back by the LP. An LP device capable of receiving in-line power will loop back the special FLP pulses when it is in a powered-down state. This is reported when MII Register 23E.9:8 = 01. If enabled, an interrupt on the $\overline{\text{MDINT}}$ pin will also be asserted. This can be verified as an in-line power detection interrupt by reading MII Register 26.9 = 1, which will subsequently be cleared and the interrupt de-asserted after the read. If an LP device does not loop back the special FLP after a specific time, then MII Register 23E.9:8 = 10.
4. If the PHY reports that the LP needs in-line power, then the Ethernet switch needs to enable in-line power on this port external of the PHY.
5. The PHY automatically disables in-line powered device detection after Event #3 above and now changes to the normal Auto-negotiation process. A link is then auto-negotiated and established when the link status register is set (MII Register bit 1.2 = 1).
6. In a link down event (MII Register bit 1.2 = 0), the in-line power should be disabled to the in-line powered device external to the PHY. The PHY will disable the normal auto-negotiation process and re-enable in-line powered device detection mode.

17.4 IEEE 802.3af (DTE Power via MDI)

The VSC8211 is fully compatible with switch designs which are intended for use in systems that supply power to the DTE (Data Terminal Equipment) via the MDI (Media Dependent Interface, or twisted pair cable), as specified by IEEE 802.3af standard (Clause 33).

18 Advanced Test Modes

18.1 1000BASE-T Ethernet Packet Generator (EPG)

For system-level debugging and in-system production testing, the VSC8211 includes an Ethernet packet generator. This can be used to isolate problems between the MAC and PHY and between a local PHY and remote link partner. It is intended for use with lab testing equipment or in-system test equipment only, and should not be used when the VSC8211 is connected to a live network.

To use the EPG, it must be enabled by writing a “1” to Extended MII Register 29E.15. This effectively disables all MAC-interface transmit pins and selects the EPG as the source for all data transmitted onto the VSC8211 media interface. For this reason, packet loss will occur if the EPG is enabled during transmission of packets from MAC to PHY. The MAC receive pins will still be active when the EPG is enabled, however. If it is necessary to disable the MAC receive pins as well, this can be done by writing a “1” to MII Register bit 0.10.

When a “1” is written to Extended MII Register Bit 29E.14, the VSC8211 will begin transmitting IEEE802.3 layer-2 compliant packets with a data pattern of repeating 16-bit words as specified in Extended MII Register 30E. The source and destination addresses for each packet, packet size, interpacket gap, FCS state, and transmit duration can all be controlled through Extended MII Register 29E. Note that if Extended MII Register Bit 29E.13 is cleared, Extended MII Register Bit 29E.14 will be cleared automatically after 30,000,000 packets have been transmitted.

18.2 1000BASE-T CRC Counter

When the EPG is enabled, a bad-CRC counter is also available for all incoming packets. This counter is available in Extended MII Register Bits 23E.7:0 - CRC Counter and is automatically cleared when read.

18.3 Far-end Loopback

Far-end loop back mode, when enabled (MII Register bit 23.3 = 1), forces incoming data from a link partner on the current media interface to be retransmitted back to the link partner on the media interface as shown in the figure below. In addition, the incoming data will also appear on the receive data pins of the MAC interface. Data present on the transmit pins of the MAC interface are ignored in this mode. This loop back mode is available in both Serial and Parallel MAC PHY operating modes. For more information, refer to “Register 23 (17h) – PHY Control Register #1” on page 108.

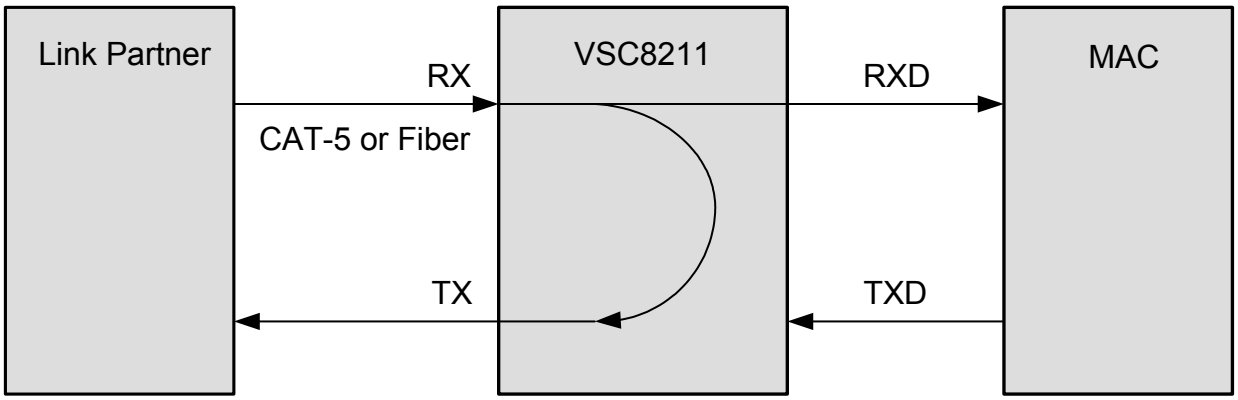


Figure 31. Far-end Loopback Block Diagram

18.4 Near-end Loopback

When Near-end loop back is set (MII Register bit 0.14 = 1), the Transmit Data (TXD) on the MAC interface is looped back onto the Receive Data (RXD) pins to the MAC as shown in the figure below. In this mode, no signal is transmitted over the network media. This loop back mode in available in both Serial MAC and Parallel MAC PHY Operating modes.

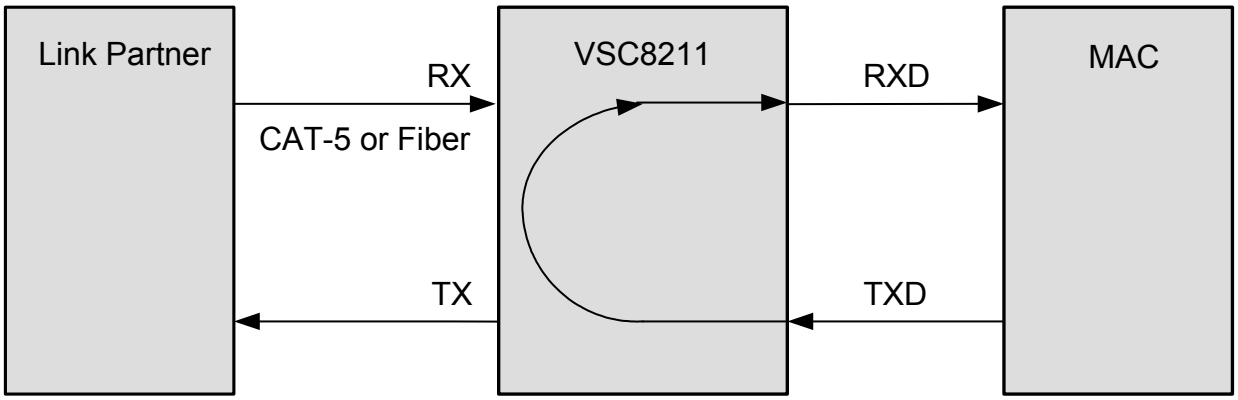


Figure 32. Near-end Loopback Block Diagram

18.5 Connector Loopback

Connector Loopback allows for the twisted pair interface to be looped back externally. In this mode the PHY must be connected to a loopback connector or a loopback cable. For this loopback, pair A should be connected to pair B and pair C to pair D. This loopback will work in all speeds selected for the interface.

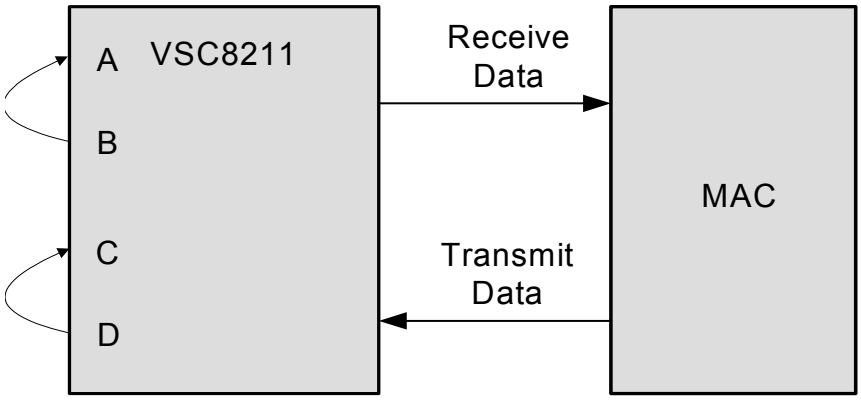


Figure 33. Connector Loopback Block Diagram

The autonegotiation, speed, and duplex can be configured using MII registers 0,4 and 9. For 1000BT connector loopback only the following additional writes are required in the specific order.

1. Master/Slave configuration forced to Master (MII Register Bits 9.12:11 = 11)

2. Enable 1000BT connector loopback (MII Register 24.0 = 1)

3. Disable pair swap correction (MII Register Bit 18.5=1)

4. Disable autonegotiation and force 1000BT link (MII Register Bit 0.12=0, MII Register Bit 0.6=1, and MII Register Bit 0.12=0) and force either full or half duplex (MII Register Bit 0.8=0 or 1).

This loopback is also available in the 100BASE-FX mode.

19 Hardware Configuration Using CMODE Pins

Each of the eight CMODE pins (CMODE[7:0]) are used to latch a four bit value at PHY reset. A total of thirty two CMODE configuration bits are set at reset. Each CMODE bit represents the default value of a particular PHY register and therefore sets a default PHY operating conditions at startup.

19.1 Setting the CMODE Configuration Bits

The CMODE bits are set by connecting each CMODE pin to either VDD33A or VSSS (ground) through an external 1% resistor. The four bit value latched by the PHY on each CMODE pin depends upon the value of the resistor used to pull-up or pull-down the CMODE pin. CMODE resistor values and connections are defined in the following table:

Table 25. CMODE Pull-up/Pull-down Resistor Values

CMODE bit 3 value	CMODE bit 2 value	CMODE bit 1 value	CMODE bit 0 value	CMODE Resistor Value	Tied to VDD33A or GND
0	0	0	0	0	GND
0	0	0	1	2.26k	GND
0	0	1	0	4.02k	GND
0	0	1	1	5.90k	GND
0	1	0	0	8.25k	GND
0	1	0	1	12.1k	GND
0	1	1	0	16.9k	GND
0	1	1	1	22.6k	GND
1	0	0	0	0	VDD33A
1	0	0	1	2.26k	VDD33A
1	0	1	0	4.02k	VDD33A
1	0	1	1	5.90k	VDD33A
1	1	0	0	8.25k	VDD33A
1	1	0	1	12.1k	VDD33A
1	1	1	0	16.9k	VDD33A
1	1	1	1	22.6k	VDD33A

19.2 CMODE Bit descriptions

The following table outlines the mapping of each CMODE bit to a PHY operating condition parameter. Each of the PHY operating condition parameters is described in detail in Table 27: “PHY Operating Condition Parameter Description”.

Table 26. CMODE Bit to PHY Operation Condition Parameter Mapping

CMODE Pin Name	'CMODE Bit' to 'PHY Operating Condition Parameter' Mapping			
	Bit 3	Bit 2	Bit 1	Bit 0
CMODE0	PHY Address[3]	PHY Address[2]	PHY Address[1]	PHY Address[0]
CMODE1	SFP Mode Disable	PHY Address[4]	SIGDET pin direction	SerDes Line Impedance
CMODE2	PHY Operating Mode[3]	PHY Operating Mode[2]	PHY Operating Mode[1]	PHY Operating Mode[0]
CMODE3	LED Control[1]	SQE Enable	10BASE-T Echo On	Auto-negotiation Advertisement Control[1]
CMODE4	LED Control[0]	Pulsing Enable	Auto-negotiation Advertisement Control[0]	MII Register View
CMODE5	RGMII/RTBI Transmit Path Timing compensation[1]	RGMII/RTBI Transmit Path Timing compensation[0]	RGMII/RTBI Receive Path Timing compensation[1]	RGMII/RTBI Receive Path Timing compensation[0]
CMODE6	PICMG Miser Mode Enable	SIGDET pin Polarity	Enhanced ActiPHY™ Enable	CLKOUTMICRO Frequency
CMODE7	Linkxxxx/Act Behaviour	Link Speed Auto-Downshift Enable	Flow Control[1]	Flow Control[0]

Each of the PHY Operating Condition Parameters mentioned in the Table 26 above is described in detail in Table 27.

Table 27. PHY Operating Condition Parameter Description

PHY Operating Condition Parameter Name	CMODE Pin Name and Bit Position	Value	Description
PHY Address[4:0]	CMODE1[2],CMODE0[3:0]	31-0	Sets the PHY Address used to access the PHY Registers when the PHY's SMI is in IEEE mode. The value latched is reflected in Register 23E (17h) - Extended PHY Control Register #4, page 129, bits 23.15:11.
PHY Operating Mode[3:0]	CMODE2[3:0]	These CMODE bits set the default PHY Operating Mode by setting the default values of MII Register 23 bits 15:12 and 2:1. For more information, see Register 23 (17h) – PHY Control Register #1, page 108.	
		0000	802.3z SerDes to CAT5 Media, Clause 37 auto-negotiation auto-sense enabled.
		0001	RGMII with Copper/Fiber Auto Media Sense (Fiber Preference).
		0010	GMII to Fiber.
		0011	GMII/MII with Copper/Fiber Auto Media Sense (Fiber Preference).
		0100	802.3z SerDes to CAT5 Media, Clause 37 disabled.
		0101	SGMII to CAT5 Media, SCLK enabled.
		0110	RGMII to CAT5 Media.
		0111	RGMII to Fiber Media.
		1000	GMII/MII to CAT5 Media.
		1001	TBI to CAT5 Media, Clause 37 auto-negotiation auto-sense enabled.
		1010	802.3z SerDes to CAT5 Media, Media Converter Mode.
		1011	TBI to Fiber Media.
		1100	RTBI to CAT5 Media, Clause 37 auto-negotiation auto-sense enabled.
		1101	Serial MAC to Fiber Media, SCLK enabled.
		1110	802.3z SerDes to CAT5 Media, Clause 37 enabled.
		1111	SGMII to CAT5 Media, SCLK disabled.
LED Control[1:0]	CMODE3[3],CMODE4[3]	This sets the default behavior of the LED pins LED[4:0] by setting the startup values of MII "Register 27 (1Bh) – LED Control Register" on page 117.	
		00	LED[4:0] = {Duplex/Collision, Link/Activity, Link10/Activity, Link100/Activity, Link1000/Activity}(MII Reg 27 = 0000h)
		01	LED[4:0] - {Activity, Duplex/Collision, Duplex/Collision, Link10/100/Activity, Link/Activity} (MII Reg 27 = 5540h)
		10	LED[4:0] - {Link Fault, Fiber Media Selected, Link/Activity, Link/Activity, Fault} (MII Reg 27 = AA80h)
		11	LED[4:0] - {Tx, Rx, Tx, Link100/1000/Activity, Rx} (MII Reg 27 = FFC0h)
Pulsing Enable	CMODE4[2]	This sets the default power saving mode of the LED pins LED[4:0] by setting the startup value of MII Register bit 27.4	
		1	Enable 5Khz, 20% duty cycle LED pulsing for power savings
		0	LED pulsing disabled

Table 27. PHY Operating Condition Parameter Description *(continued)*

PHY Operating Condition Parameter Name	CMODE Pin Name and Bit Position	Value	Description
Link/Activity and Linkxxxx/Activity behaviour	CMODE7[3]	This sets the LED behaviour by setting the default values of MII Register 27.2:1 .	
		1	Link function indicated link status only.
		0	All link function blinks or flashes when activity is present. Blink or flash behavior is selected by the Blink/Pulse-stretch Enable and Blink/Pulse-stretch rate bits.
RGMII/RTBI Transmit Path Timing Compensation[1:0]	CMODE5[3:2]	Sets the RGMII/RTBI Transmit Path Timing compensation. This timing compensation adds a configurable delay to the signal on the TXC pin. These CMODE bits set the default value of MII Register 23.11:10.	
		00	2.0ns
		01	2.5ns
		10	No skew
		11	1.5ns
RGMII/RTBI Receive Path Timing Compensation[1:0]	CMODE5[1:0]	Sets the RGMII/RTBI Receive Path Timing compensation. This timing compensation adds a configurable delay to the RXC signal internal to the chip. These CMODE bits set the default value of MII Register 23.9:8.	
		00	2.0ns
		01	2.5ns
		10	No skew
		11	1.5ns
Auto-negotiation Advertisement Control[1:0]	CMODE3[0],CMODE4[1]	These CMODE bits set the default auto-negotiation advertisement by setting the initial values of MII Registers 4 and 9.	
		00	10/100/1000BASE-T HDX, 10/100/1000BASE-T FDX
		01	10/100BASE-T HDX, 10/100/1000BASE-T FDX
		10	10/100BASE-T HDX, 10/100BASE-T FDX
		11	1000BASE-T FDX
Flow Control[1:0]	CMODE7[1:0]	00-11	Sets the default value of the Flow Control bits of MII Register 4. The value on these CMODE pins is the default value of MII Register 4.11:10 in Clause 28 Register View Mode and the default value of MII Register 4.8:7 in Clause 37 Register View Mode. The MII Register View is set by CMODE bit CMODE4[0] (page 70).

Table 27. PHY Operating Condition Parameter Description *(continued)*

PHY Operating Condition Parameter Name	CMODE Pin Name and Bit Position	Value	Description
SFP Mode Disable	CMODE1[3]	This CMODE bit sets the default value of MII Register 21E.15.	
		0	This sets MII Register 21E.15 = 1. Sets the following PHY defaults: • TXDIS/$\overline{\text{SRESET}}$ is active high i.e. behaves like TXDIS. • MODDEF0/CLKOUTMAC pin functions like MODDEF0 i.e this pin is asserted low by the PHY once the EEPROM interface is released for access through the SMI interface. • RXLOS/SIGDET pins functions like the RXLOS. • The SMI interface is set in MSA mode.
		1	This sets MII Register 21E.15 = 0. Sets the following PHY defaults: • TXDIS/$\overline{\text{SRESET}}$ is active low i.e. behaves like $\overline{\text{SRESET}}$. • MODDEF0/CLKOUTMAC pin functions like CLKOUTMAC i.e this pin drives out a 125Mhz clock. • RXLOS/SIGDET pin functions like SIGDET. • The SMI interface is set in IEEE mode.
SIGDET pin direction	CMODE1[1]	The value of this bit is valid in non-SFP mode when CMODE bit CMODE1[3] is 1. This CMODE bit sets the direction of the SIGDET pin by setting the default value of Extended MII Register 19E.1	
		0	Input
		1	Output
SerDes Line Impedance	CMODE1[0]	Sets the internal end termination resistance value of the Serial MAC/ Media Interface Input pins.	
		0	50 Ω
		1	75Ω
SQE Enable	CMODE3[2]	Sets the default value of MII Register 22.12.	
		0	SQE Disabled (MII Register 22.12 = 1)
		1	SQE Enabled (MII Register 22.12 = 0)
10BASE-T Echo On	CMODE3[1]	Sets the default value of MII Register 22.13.	
		0	10BASE-T Echo disabled (MII Register 22.13 = 1)
		1	10BASE-T Echo Enabled (MII Register 22.13 = 0)
MII Register View	CMODE4[0]	Sets the default Register View of the standard IEEE specified Registers (MII Register 0 through MII Register 15).	
		0	Clause 28 view (specified for 1000BASE-T devices)
		1	Clause 37 view (specified for 1000BASE-X devices)
PICMG Miser Mode Enable	CMODE6[3]	Sets the default value of MII Register 24.12. Putting the PHY in this mode reduces power consumption. This mode is suitable for applications where the signal to noise ratio on the CAT-5 media is high, such as ethernet over the backplane. See Section 12: "Transformerless Operation for PICMG 2.16 and 3.0 IP-based Backplanes" on page 45 for more information.	
		0	PICMG Miser Mode Disabled
		1	PICMG Miser Mode Enabled

Table 27. PHY Operating Condition Parameter Description *(continued)*

PHY Operating Condition Parameter Name	CMODE Pin Name and Bit Position	Value	Description
SIGDET pin Polarity	CMODE6[2]	The value of this bit is valid in non-SFP mode i.e. when CMODE bit CMODE1[3] is 1. This CMODE bit sets the polarity (active high or active low) of the SIGDET pin by setting the default value of Extended MII Register 19E.0.	
		0	Active High
		1	Active Low
Enhanced ActiPHY™ Enable	CMODE6[1]	This CMODE bit sets the default value of MII Register 28.6.	
		0	Enhanced ActiPHY™ Mode Disabled
		1	Enhanced ActiPHY™ Mode Enabled
CLKOUTMICRO Frequency	CMODE6[0]	This bit sets the default value of Extended MII Register 20E.8.	
		0	4Mhz
		1	125 MHz
Link Speed Auto-Downshift Enable	CMODE7[2]	Sets the default value of Extended MII Register 20E.4.	
		0	Link Speed Auto-Downshift Disabled
		1	Link Speed Auto-Downshift Enabled

19.3 Procedure For Selecting CMODE Pin Pull-up/Pull-down Resistor Values

1. Using the descriptions in Table 27 column D (“Description”), choose the desired PHY operating condition parameter values from Column C (“Value”).
2. Using Table 27 Column B (“CMODE Pin Name and Bit Position”) and the chosen PHY operating condition parameter values, enter the value of each CMODE pin in Table 26: “CMODE Bit to PHY Operation Condition Parameter Mapping”.
3. Choose the value of each CMODE pull-up or pull-down resistor from Table 25: “CMODE Pull-up/Pull-down Resistor Values” based on the CMODE Bit values in Table 26.

20 EEPROM Interface

The EEPROM Interface consists of the EEDAT and EECLK pins of the PHY. If this interface is used, these pins should connect to the SDA and SCL pins respectively of a serial EEPROM that is compatible with the AT24xxx series of ATMEL EEPROMs.

The EEPROM interface on the VSC8211 serves the following purposes:

- It provides the PHY with the ability to self configure its internal registers.
- The system manager can access the EEPROM to obtain information pertaining to the system/module configuration.
- A single EEPROM can be shared among multiple PHYs for their custom configuration.

The PHY detects the EEPROM based on the presence of a pull-up on the EEDAT pin. It is initialized using the configuration EEPROM (if present) under the following conditions:

- $\overline{\text{RESET}}$ deassertion.
- TXDIS/$\overline{\text{SRESET}}$ deassertion and Extended MII Register 21E.14 is set.
- S/W reset (MII Register 0.15) is asserted and Extended MII Register 21E.14 is set.

If an EEPROM is present, the start-up control block looks for a “Vitesse Header” (value:16’hBDBD’) at addresses 0 and 1 of the EEPROM. The address is incremented by 256 until the Vitesse Header is found. If the Vitesse Header is not found, or no EEPROM is connected, the VSC8211 bypasses the EEPROM read step.

Once the Vitesse header is located, the EEPROM Interface block of the PHY searches for its PHY address in bit position 7:3 in the subsequent EEPROM locations. Once the PHY address is located, the 11 bit EEPROM address location for the start of the configuration script is read. At this point, the PHY begins reading from this 11 bit EEPROM address and initializes its Register values based on the EEPROM configuration script contents. For more information see Table 28, “Configuration EEPROM Data Format,” on page 73.

The total number of EEPROM bytes needed for a configuration script is equal to:

((Number of Register writes) * 3 + 2 (BDBD) + 2 (PHY address and Configuration Script Address) + 2 (Length of configuration script)).

Data is read from the EEPROM sequentially (at 50 Khz, or 50 kbits/s) until all PHY Register are set. Once all of the PHY registers are set, the PHY enters the ‘NORMAL STATE’ (Section 21: "PHY Startup and Initialization").

If the PHY is in ‘NORMAL STATE’ state, the user can access the EEPROM connected to the EEPROM interface through the SMI. If the SMI is in IEEE mode, the EEPROM can be accessed via the SMI using Extended MII Registers 21E and 22E. If the SMI is in MSA mode, the EEPROM can be accessed directly via the SMI i.e. the PHY behaves as if the MODDEF2 and MODDEEF1 pins of the SMI are directly connected to the EEDAT and EECLK pins of the PHY.[1]

One exception is the memory portion with device/page address ‘110’. This is reserved for the PHY Register access when the PHY’s SMI is set in MSA mode.

If an EEPROM is present, but the EEPROM does not acknowledge (according to the ATMEL EEPROM protocol), the VSC8211 waits for an acknowledge for approximately 3 seconds. If there is no acknowledge within 3 seconds, the VSC8211 will abort and continue into normal operation.

[1]EEPROM memory with device address ‘110’ cannot be accessed directly when the SMI is in MSA mode. This device address is reserved for PHY Register access in MSA mode. To access EEPROM with device address ‘110’ in MSA mode Extended MII Registers 21E and 22E should be used.

20.1 Programming Multiple VSC8211s Using the Same EEPROM

To prevent contention on the 2 wire bus when multiple PHYs use the same EEPROM for initialization, the EEPROM start-up block of each VSC8211 monitors the bus for (PHY Address[4:0] + 1) * 9 + 92 clock cycles for no bus activity and only then attempts to access the EEPROM bus. PhyAddress[4:0] is chosen because these are the PHY Address bits that are unique to each VSC8211. (i.e VSC8211 with lowest PHY Address gets priority on this bus.)

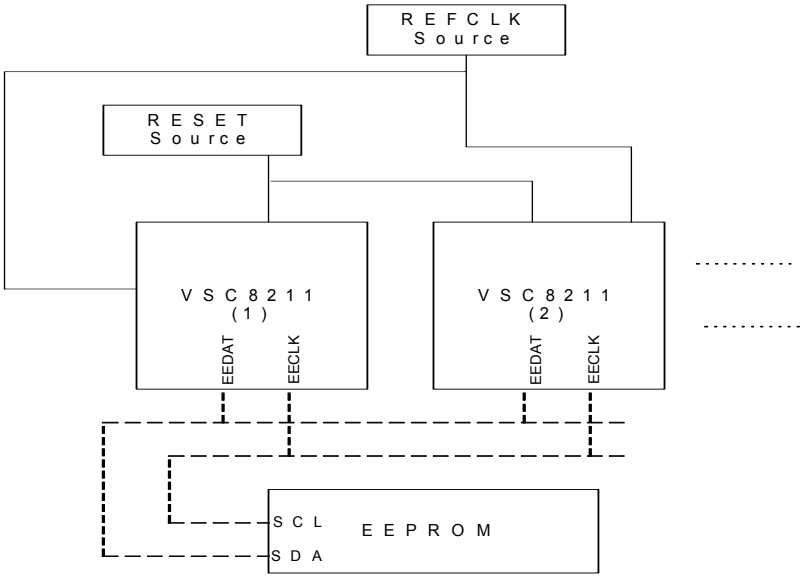


Figure 34. EEPROM Interface Connections

NOTE: The same clock must be used for each VSC8211's REFCLK input. In addition, the $\overline{\text{RESET}}$ pin for each VSC8211 must be driven from the same source to ensure that the reference clock modes within each device are correctly set.

This prevents using the CLKOUTMAC or CLKOUTMICRO output from one VSC8211 to drive the clock input of another VSC8211, if the devices are sharing the same EEPROM.

Table 28. Configuration EEPROM Data Format

Address	Contents
----------	----------
----------	----------
----------	----------
----------	----------
O+7	Data to be written (LSB)
O+6	Data to be written (MSB)
O+5	RegAddress b
O+4	Data to be written (LSB)
O+3	Data to be written (MSB)
O+2	RegAddress a
O+1	Number of PHY Register writes *3[7:0]
{bpage_addr3,s_addr3} = O	Number of PHY Register writes *3[15:8]

Table 28. Configuration EEPROM Data Format *(continued)*

Address	Contents
----------	----------
----------	----------
----------	----------
----------	----------
M+7	Data to be written (LSB)
M+6	Data to be written (MSB)
M+5	RegAddress b
M+4	Data to be written (LSB)
M+3	Data to be written (MSB)
M+2	RegAddress a
M+1	Number of PHY Register writes *3[7:0]
{bpage_addr2,s_addr2} = M	Number of PHY Register writes *3[15:8]
----------	----------
N+7	Data to be written (LSB)
N+6	Data to be written (MSB)
N+5	RegAddress b
N+4	Data to be written (LSB)
N+3	Data to be written (MSB)
N+2	RegAddress a
N+1	Number of PHY Register writes *3[7:0]
{bpage_addr1,s_addr1} = N	Number of PHY Register writes *3[15:8]
----------	----------
7,263,519,..	Starting address for initializing PHY3 s_addr3
6,262,518,..	{PHY Address 1[4:0], 3’bpage_addr3}
5,261,517,..	Starting address for initializing PHY2 s_addr2
4,260,516,..	{PHY Address 2[4:0], 3’bpage_addr2}
3,259,515,..	Starting address for initializing PHY1 s_addr1
2,258,514,..	{PHY Address 1[4:0], 3’bpage_addr1}
1,257,513..	8’hBD
0,256,512...	8’hBD

Using the EEPROM data format shown in Table 28 enables multiple PHYs to be initialized in a similar way by reading the same locations from the EEPROM. If the PHYs have to be initialized differently, then the 'Address pointers' will differ for each PHY, along with different PHY configuration data values.

21 PHY Startup and Initialization

The PHY Startup and Initialization sequence is detailed in the flowchart below.

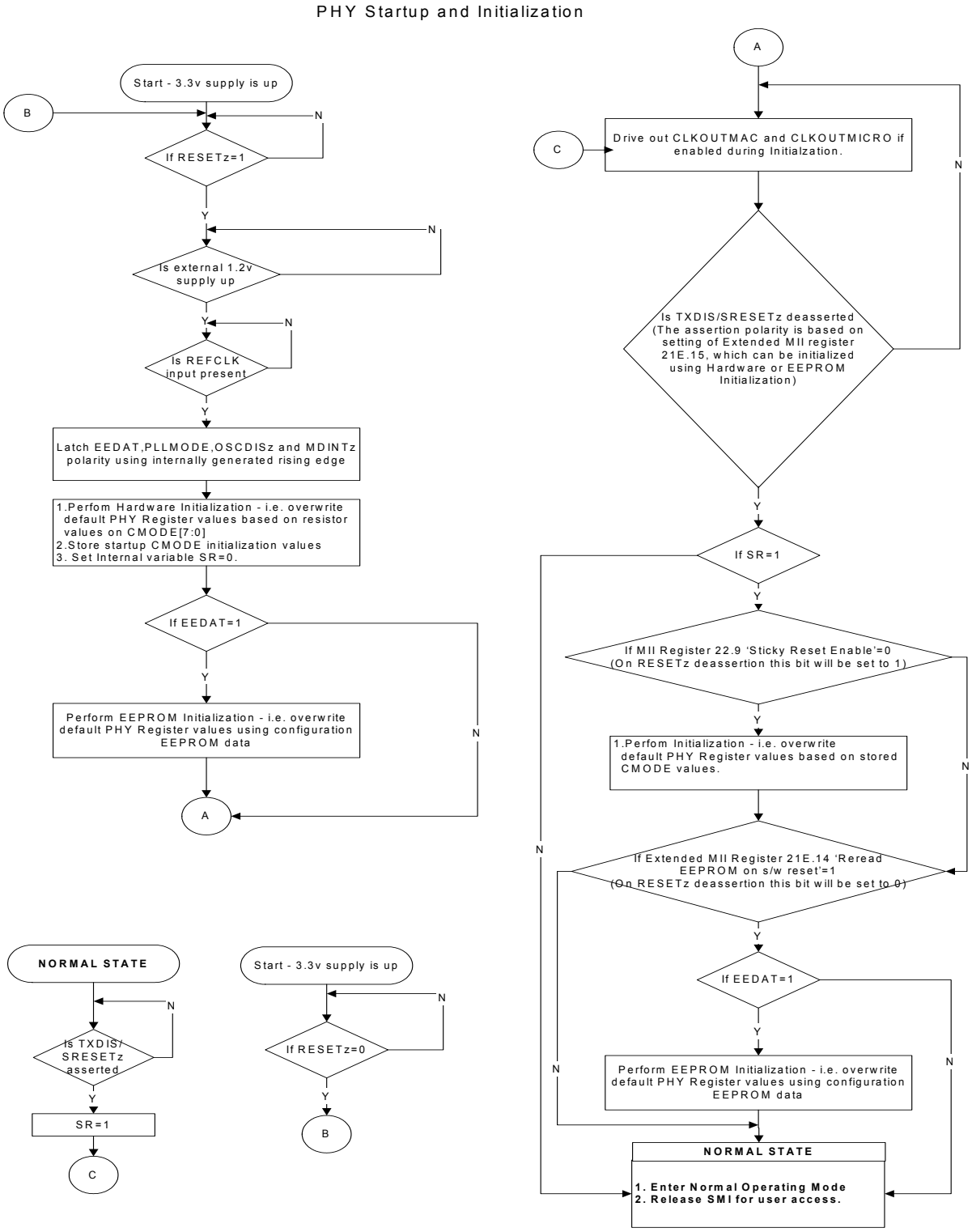


Figure 35. PHY Startup and Initialization Sequence

22 PHY Operating Modes

The PHY Operating Mode is set according to the value of MII Register 23.15:12,23.2:1. Refer to Section 19: "Hardware Configuration Using CMODE Pins" and Section 20: "EEPROM Interface" for details on PHY Operating Mode configuration at startup. The following table summarizes the PHY operating modes.

Table 29. PHY Operating Modes

Operating Mode Category	MII Register 23.15:12,23.2:1	CMODE2 [3:0]	MAC Interface	Media Interface	Other Settings
Parallel MAC PHY Operating Modes	0011, 10	1000	GMII/MII	CAT5	
	0011, 01	0010	GMII	Fiber	
	0010, 01	0011	GMII/MII	Auto Media Sense	Fiber Preference
	0010, 10	-	GMII/MII	Auto Media Sense	CAT5 Preference[1]
	0001, 10	0110	RGMII	CAT5	
	0001, 01	0111	RGMII	Fiber	
	0000, 01	0001	RGMII	Auto Media Sense	Fiber Preference
	0000, 10	-	RGMII	Auto Media Sense	CAT5 Preference[1]
	0110, 00	1001	TBI	CAT5	With Clause 37 Auto-Negotiation Detection
	0111, 01	1011	TBI	Fiber[2]	
	0100, 00	1100	RTBI	CAT5	With Clause 37 Auto-Negotiation Detection
	0101, 01	-	RTBI	Fiber[2]	
Serial MAC PHY Operating Modes	1111, 00	0100	802.3z SerDes	CAT5	Clause 37 disabled
	1110, 01	1110	802.3z SerDes	CAT5	Clause 37 enabled
	1110, 10	1010	802.3z SerDes	CAT5	Clause 37 enabled, Media Convertor Mode
	1110, 00	0000	802.3z SerDes	CAT5	With Clause 37 Auto-Negotiation Detection
	1010, 01	1111	SGMII	CAT5	625Mhz SCLK Clock Disabled
	1000, 01	0101	SGMII	CAT5	625MHz SCLK Clock Enabled
	1001, 01	1101	Serial	Serial	Buffered Mode – With Clock Recovery[3]
	1001, 00		SGMII	CAT5	Modified Clause 37 auto-negotiation disabled, 625MHz SCLK Clock Enabled
	1011, 00		SGMII	CAT5	Modified Clause 37 auto-negotiation disabled, 625MHz SCLK Clock Disabled

[1] In this mode the PHY does not drop the Fiber Media link if the CAT5 link comes up after the Fiber link has been established and therefore it is not a suitable mode for unmanaged applications. For more information on how to use this mode in managed applications, contact you Vitesse Semiconductor representative.
[2] PHY Registers are not supported in this mode.
[3] In this mode, the PHY's MAC and media interfaces are the same. Both interfaces can be either SGMII or 802.3z SerDes.

22.1 PHY Operating Mode Description

Most of the PHY Operating Modes listed in Table 29: "PHY Operating Modes" are standard operating modes. Some of the non-standard modes are described below:

22.1.1 Auto Media Sense (AMS) Media Interface PHY Operating Modes

The VSC8211 can be configured for GMII/MII to AMS or RGMII to AMS Media Interface PHY Operating Modes. In these modes, the PHY continuously tries to establish a link on both the CAT5 and Fiber medias. When a link is established on the preferred media, the PHY turns off the non-preferred media interface.

22.1.2 Serial MAC to Serial Media PHY Operating Mode:

In this mode, the high-speed serial data on the SDIP/SPIN input pins is routed to the RDP/RDN output pins and data from the TDP/TPN input pins is routed to the SDOP/SDON output pins. A 625MHz clock, recovered from the data on the SDIP/SDIN input pins, is driven out on the SCLKP/SCLKN outputs.

See Section 9.4.10: "Serial MAC/Media Interface Signals" for more information.

23 IEEE802.3 Clause 28/37 Remote Fault Indication Support

The VSC8211 is capable of both Clause-28 and Clause-37 autonegotiation. In addition, the VSC8211 can be configured for a register view corresponding to Clause-28 or Clause-37. However, in IEEE802.3, Clause-37 provides for two remote fault bits, while Clause-28 provides only a single remote fault bit. A third remote fault status bit is also located in MII Register Bit 1.4, which is independent of the register view.

In instances where the register view is configured for a different IEEE Clause than the current autonegotiation advertisement, Extended MII Register -bits 16E.2:0 handle the mapping between autonegotiation and register view. These bits also control the result of MII Register bit 1.4 if a remote fault is detected in the link partner.

There are four possible combinations of register view and autonegotiation. In each case, remote fault conditions are both transmitted by the local PHY and received from the link partner. Remote fault conditions in each of these are described below:

Clause-28 autonegotiation with Clause-28 register view- One remote fault bit is received from the link partner and one bit is transmitted from the local PHY to the link partner. No special handling of registers 4/5, or MII Register bit 1.4 is necessary, as the two modes are identical.

Clause-28 autonegotiation with Clause-37 register view- One remote fault bit is received from the link partner and must be mapped to two MII Register bits 5.13:12, as well as MII Register bit 1.4. Two remote fault MII Register bits 4.13:12 must be mapped to a single bit to transmit from the local PHY to the link partner.

Clause-37 autonegotiation with Clause-28 register view- Two remote fault bits are received from the link partner and must be mapped to one MII Register bit 5.13, as well as MII Register bit 1.4. One remote fault MII Register bit 4.13 must be mapped to two bits to transmit from the local PHY to the link partner.

Clause-37 autonegotiation with Clause-37 register view- Two remote fault bits are received from the link partner and two remote fault bits are transmitted from the local PHY to the link partner. No special handling of registers 4/5 is necessary. MII Register bits 5:13:12 must be mapped to MII Register bit 1.4.

Extended MII Register 16E bits 2:1, the Remote Fault Mapping Mask, and bit 0, the Remote Fault Mapping OR, handle remote fault mapping. For more information, see Register 16E (10h) – Fiber Media Clause 37 Autonegotiation Control & Status, page 123. The functionality of these bits is summarized in the following tables:

Table 30. Clause 28 Register View Remote Fault Transmitted to Link Partner

Bit 4.13, Local Remote Fault	Bit 16E.0, Remote Fault OR	Bits 16E.2:1, Remote Fault Mask	Value Transmitted to LP during Clause-28 Autonegotiation (combination 1, above)	Value Transmitted to LP during Clause-37 Autonegotiation (combination 3, above)
0	x	xx	0	00
1	x	xx	1	Equal to bits 16E.2:1

Table 31. Clause 37 Register View Remote Fault Transmitted to Link Partner

Bits 4.13:12, Local Remote Fault	Bit 16E.0, Remote Fault OR	Bits 16E.2:1, Remote Fault Mask	Value Transmitted during Clause-28 Autonegotiation (combination 2, above)	Value Transmitted during Clause-37 Autonegotiation (combination 4, above)
00	0	00	0	00
01, 10 or 11	0	01, 10 or 11	1, if bits 4.13:12 equal bits 16E.2:1 0, if bits 4.13:12 do not equal bits 16E.2:1	Equal to bits 4.13:12
01, 10 or 11	1	xx	1	Equal to bits 4.13:12

Table 32. Clause 28 Autonegotiation Link Partner Remote Fault

LP Remote Fault Bit[1]	Bit 16E.0, Remote Fault OR	Bits 16E.2:1, Remote Fault Mask	Value Displayed in Clause-28 View Register Bit 1.4	Value Displayed in Clause-37 View Register Bit 1.4	Value Displayed in Clause-28 View Register Bit 5.13 (combination 1, above)	Value Displayed in Clause-37 View Register Bits 5.13:12 (combination 2, above)
0	x	xx	0	0	0	00
1	x	00	1	0	1	00
1	x	01, 10 or 11	1	1	1	Equal to bits 16E.2:1

[1] This is the remote fault bit sent by the link partner during Clause-28 autonegotiation

Table 33. Clause 37 Autonegotiation Link Partner Remote Fault

LP Remote Fault Bits[1]	Bit 16E.0, Remote Fault OR	Bits 16E.2:1, Remote Fault Mask	Value Displayed in Register Bit 1.4	Value Displayed in Clause-28 View Register Bit 5.13 (combination 3, above)	Value Displayed in Clause-37 View Register Bits 5.13:12 (combination 4, above)
00	x	xx	0	0	00
01, 10 or 11	0	xx	1, if LP remote fault bits equal bits 16E.2:1 0, if LP remote fault bits do not equal bits 16E.2:1	1, if LP remote fault bits equal bits 16E.2:1 0, if LP remote fault bits do not equal bits 16E.2:1	Equal to LP remote fault bits
01, 10 or 11	1	xx	1	1	Equal to LP remote fault bits

[1] These are the remote fault bits sent by the link partner during Clause-37 autonegotiation

24 PHY Register Set Conventions

The user can control the PHY's features, operating modes, etc. by setting the PHY Registers to the desired values. The PHY provides access to its Registers via the Serial Management Interface. For details on PHY Register access, see Section 13 “Dual Mode Serial Management Interface (SMI),” page 45.

24.1 PHY's Register Set Structure

The register access protocol, as defined by the IEEE 802.3 specification, reserves five bits for register addressing. This limits the register space to 32, 16 bit wide registers. Of these, registers addressed 0 through 15 are defined by the IEEE 802.3 specification and registers addressed 16 through 31 are vendor specific. To provide extensive feature control of the PHY, the vendor specific registers addressed 16 through 31 have been divided into two Page views, called PAGE0 and PAGE1, enabling access to 32 vendor specific registers instead of 16.

PAGE0 is the default page view. To switch to PAGE1, write 0001h to PHY Register 31. To switch to PAGE0 write 0000h to PHY Register 31.

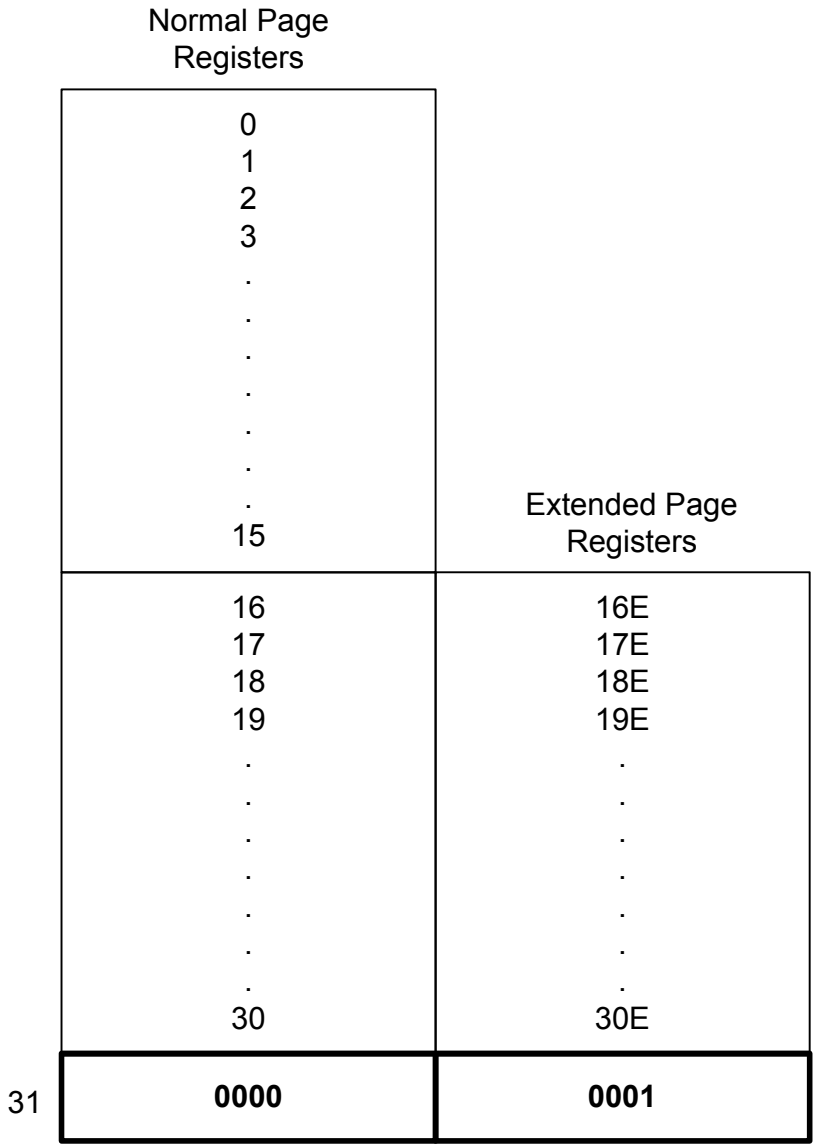


Figure 36. Extended Page Register Diagram

24.2 PHY's Register Set Nomenclature

Register Address	Page View	Naming Convention
0-15	- NA-	MII Register
16-31	PAGE0	MII Register
16-31	PAGE1	Extended Page MII Register (Referred to with an 'E' after the register number e.g. 20E.15 is Page 1 Register 20 bit 15)

24.3 PHY Register Bit Types

PHY Register bit types are defined in the table below:

Register Bit Type	Description
R/W	Read and Write, effective immediately
RO	Read Only (must be written '0', unless specified otherwise)
RO SC	Read Only, Self Clears after Read
LH	Latched High, Clears after Read
LL	Latched Low, Clears after Read
SC	Self-Cleared
RWSW	Read and Write, effective after s/w reset. This register will read the new value only after s/w reset.

"Sticky" refers to the behavior of the register bit(s) after a software reset. If an "S" appears in the sticky column, the corresponding bit(s) will retain their values after a software reset, as long as the correct MII register bit is set. For more information, see Section 25.3.23 "Register 22 (16h) – Control & Status Register," page 106.

If an "SS" appears in the sticky column, the corresponding bit(s) will retain their values after a software reset, regardless of the state of the register bit.

25 PHY Register Set

25.1 Clause 28/37 Resister View

PHY registers 0 through 15 are implemented according to the IEEE 802.3 specification. According to this standard, the contents of MII Registers 4, 5, 6, 9 and 10 are different for 1000BASE-X PHYs and 1000BASE-T PHYs. Since the VSC8211 supports both Fiber (1000BASE-X) and CAT5 (1000BASE-T) media, it supports both register sets.

In registers 0 through 15, the 1000BASE-T register set is referred to as the “Clause 28 View” and the 1000BASE-X register set is referred to as the “Clause 37 View”.

The default register view is “Clause 28 View” for all PHY Operating Modes. To switch the Register View to “Clause 37 View”, set the “Register View” bit (MII Register 23.4). Refer to section 19, “Hardware Configuration Using CMODE Pins,” page 66, and section 20, “EEPROM Interface,” page 72 for details on Register View configuration at startup.

- Please note that “Clause 37" Register View is allowed only in 'GMII/RGMII to CAT5/Fiber/AMS' category of PHY operating modes i.e. where MII Register 23.15:12,23.2:1 = 6'b00xxxx.

25.2 PHY Register Names and Addresses

Table 34. PHY Register Names and Addresses

Register Name	Register Number	Register Address (hex)
Mode Control	0	00
Mode Status	1	01
PHY Identifier Register # 1	2	02
PHY Identifier Register # 2	3	03
Auto-Negotiation Advertisement	4	04
Auto-Negotiation Link Partner Ability	5	05
Auto-Negotiation Expansion	6	06
Auto-Negotiation Next-Page Transmit	7	07
Auto-Negotiation Link Partner Next Page Receive	8	08
1000BASE-T Control	9	09
1000BASE-T Status Register # 1	10	0A
Reserved	11	0B
Reserved	12	0C
Reserved	13	0D
Reserved	14	0E
1000BASE-T Status Register #2	15	0F
Reserved	16	10
Reserved	17	11
Bypass Control	18	12
Reserved	19	13
Reserved	20	14
Reserved	21	15
Control & Status	22	16
PHY Control # 1	23	17
PHY Control # 2	24	18
Interrupt Mask	25	19
Interrupt Status	26	1A
LED Control	27	1B
Auxiliary Control & Status	28	1C
Reserved	29	1D
MAC Interface Clause 37 Autonegotiation Control & Status	30	1E
Extended Page Access	31	1F
Fiber Media Clause 37 Autonegotiation Control & Status	16E	10
SerDes Control	17E	11
Reserved	18E	12
SerDes Control Register # 2	19E	13
Extended PHY Control # 3	20E	14
EEPROM Interface Status and Control	21E	15
EEPROM Data Read/Write	22E	16
Extended PHY Control # 4	23E	17
Reserved	24E	18
Reserved	25E	19

Table 34. PHY Register Names and Addresses *(continued)*

Register Name	Register Number	Register Address (hex)
Reserved	26E	1A
Reserved	27E	1B
Reserved	28E	1C
1000BASE-T Ethernet Packet Generator (EPG) # 1	29E	1D
1000BASE-T Ethernet Packet Generator (EPG) # 2	30E	1E

25.3 MII Register Descriptions

25.3.1 Register 0 (00h) – Mode Control Register - Clause 28/37 View

Register 0 (00h) – Mode Control Register - Clause 28/37 View					
Bit	**Name**	**Access**	**States**	**Reset Value**	**Sticky**
15	Software Reset[1]	R/W SC	1 = Reset asserted 0 = Reset de-asserted	0	
14	Near End Loopback	R/W	1 = Near End Loopback on 0 = Near End Loopback off	0	
6, 13	Forced Speed Selection	R/W	00 = 10Mbps 01 = 100Mbps 10 = 1000Mbps 11 = Reserved	10	
12	Auto-Negotiation Enable	R/W	1 = Auto-Negotiation enabled 0 = Auto-Negotiation disabled	1	
11	Power-Down	R/W	1 = Power-down 0 = Power-up	0	
10	Isolate[2]	R/W	1 = Disable Parallel MAC outputs 0 = Normal Operation	0	
9	Restart Auto-Negotiation	R/W SC	1 = Restart MII 0 = Normal operation	0	
8	Duplex Mode	R/W	1 = Full duplex 0 = Half duplex	0	
7	Collision Test Enable	R/W	1 = Collision test enabled 0 = Collision test disabled	0	
6	MSB for Speed Selection (see bit 13 above)	R/W	See “Forced Speed Selection” Above	1	
5:0	Reserved	RO		000000	

[1] In MSA mode, when this bit is set, the PHY does not return the correct values for the subsequent register read operations. In order to read the correct PHY register values, the station manager must provide 70 clock cycles on the MODDEF1/MDC pin or perform two byte read operations on any eeprom address other than in page ‘110’ immediately following s/w reset.

[2] When this bit is set, while the PHY is operating in one of the ‘Serial MAC/TBI/RTBI to CAT5 Media’ category of PHY operating modes. The PHY will drop the CAT5 Media link. Also, setting of this bit will not disable the clock output on SCLKP and SCLKN pins.

0.15 – Software Reset

Writing a “1” to bit 0.15 initiates a software reset. Once Software Reset is asserted, the PHY is returned to normal operating mode and is ready for the next SMI transaction, so Software Reset always reads back “0”. Software Reset restores all SMI registers to their default states, except for registers marked with an “S” or “SS” in the sticky column.

0.14 – Near End Loopback

When the Near End Loopback bit is set, the Transmit Data (TXD) on the MAC interface is looped back onto the Receive Data (RXD) pins to the MAC. In this mode, no signal is transmitted over the network media. The loopback mechanism works in all (10/100/1000) modes of operation. The operating mode is determined by bits 0.13 and 0.6 (forced speed selection). See section 18.4, “Near-end Loopback,” page 64 for more information.

0.13, 0.6 – Forced Speed Selection

These bits determine the 10/100/1000 speed when Auto-Negotiation is disabled by clearing control bit 0.12. These bits are ignored if control bit 0.12 is set. These bits also determine the operating mode when Near End Loopback (bit 0.14) is set.

0.12 – Auto-Negotiation Enable

After a power-up, or reset, the PHY automatically activates the Auto-Negotiation state machine, setting bit 0.12 to a “1”. If a “0” is written to bit 0.12, the Auto-Negotiation process is disabled and the present contents of the PHY’s SMI register bits determine the operating characteristics. Note that Auto-Negotiation is always required in 1000BASE-T mode.

0.11 – Power-Down

Power-Down functions the same as Software Reset, except that it is not self-clearing, and that R/W SMI bits are *not* restored to their default states by Power-Down. The RGMII pins (except for SMI pins MDC, MDIO, and MDINT#) are electrically isolated during power-down. After Power-Down is released (i.e., set to “0”), the PHY will be ready for normal operation before the next SMI transaction. If Auto-Negotiation is enabled, the PHY will begin Auto-Negotiation immediately upon exiting Power-Down.

0.10 – Isolate

When Isolate is asserted (i.e., set to “1”), all MAC outputs (except for MDIO) will be high impedance. Operation of the PHY is otherwise unaffected. For example, if Isolate is asserted while Auto-Negotiation is under way, Auto-Negotiation will continue unaffected.

0.9 – Restart Auto-Negotiation

When Restart Auto-Negotiation is asserted (i.e., set to “1”), the Auto-Negotiation state machine will restart the Auto-Negotiation process, even if it is in the midst of an Auto-Negotiation process. This control bit is self-clearing, meaning that it will always return a “0” when read.

0.8 – Duplex Mode

Bit 0.8 determines the duplex mode of the VSC8211 when Auto-Negotiation is disabled. Changes to the state of Duplex Mode while Auto-Negotiation is enabled are ignored.

0.7 – Collision Test Enable

Collision Test allows the COL pin (pin B4 in GMII/MII Mode) to be tested during Near End Loopback. When Collision Test is enabled (by setting this bit), asserting TXEN will cause the COL output to go high within 512 bit times. De-asserting TXEN will cause the COL output go low within 4 bit times. The Collision Test should only be enabled when Near End Loopback is enabled.

0.5:0 – Reserved

25.3.2 Register 1 (01h) – Mode Status Register - Clause 28/37 View

Register 1 (01h) – Mode Status Register - Clause 28/37 View

Bit	Name	Access	States	Reset Value	Sticky
15	100BASE-T4 Capability	RO	1 = 100BASE-T4 capable	0	
14	100BASE-X FDX Capability	RO	1 = 100BASE-X FDX capable	1	
13	100BASE-X HDX Capability	RO	1 = 100BASE-X HDX capable	1	
12	10BASE-T FDX Capability	RO	1 = 10BASE-T FDX capable	1	
11	10BASE-T HDX Capability	RO	1 = 10BASE-T HDX capable	1	
10	100BASE-T2 FDX Capability	RO	1 = 100BASE-T2 FDX capable	0	
9	100BASE-T2 HDX Capability	RO	1 = 100BASE-T2 HDX capable	0	
8	Extended Status Enable	RO	1 = Extended status information present in R15	1	
7	Reserved	RO		0	
6	Preamble Suppression Capability	RO	1 = MF preamble may be suppressed 0 = MF preamble always required	1	
5	Auto-Negotiation Complete	RO	1 = Auto-Negotiation complete 0 = Auto-Negotiation not complete	0	
4	Remote Fault	RO LH	1 = Far-end fault detected 0 = No fault detected	0	

Register 1 (01h) – Mode Status Register - Clause 28/37 View					
Bit	**Name**	**Access**	**States**	**Reset Value**	**Sticky**
3	Auto-Negotiation Capability	RO	1 = Auto-Negotiation capable	1	
2	Link Status	RO LL	1 = Link is up 0 = Link is down	0	
1	Jabber Detect	RO LH	1 = Jabber condition detected 0 = No jabber condition detected	0	
0	Extended Capability	RO	1 = Extended register capable	1	

1.15 – 100BASE-T4 Capability

The VSC8211 is not 100BASE-T4 capable, so this bit is hard-wired to “0”.

1.14 – 100BASE-X FDX Capability

The VSC8211 is 100BASE-X FDX capable, so this bit is hard-wired to “1”.

1.13 – 100BASE-X HDX Capability

The VSC8211 is 100BASE-X HDX capable, so this bit is hard-wired to “1”.

1.12 – 10BASE-T FDX Capability

The VSC8211 is 10BASE-T FDX capable, so this bit is hard-wired to “1”.

1.11 – 10BASE-T HDX Capability

The VSC8211 is 10BASE-T HDX capable, so this bit is hard-wired to “1”.

1.10 – 100BASE-T2 FDX Capability

The VSC8211 is not 100BASE-T2 FDX capable, so this bit is hard-wired to “0”.

1.9 – 100BASE-T2 HDX Capability

The VSC8211 is not 100BASE-T2 HDX capable, so this bit is hard-wired to “0”.

1.8 – Extended Status Enable

The VSC8211 is extended status capable, so this bit is hard-wired to “1”.

1.7 – Reserved

1.6 – Preamble Suppression Capability

The VSC8211 accepts management frames on the SMI without preambles, so preamble suppression capability is hard-wired to “1”. The management frame preamble may be as short as 1 bit.

1.5 – Auto-Negotiation Complete

When this bit is a “1”, the contents of Registers 4, 5, 6, 10 and 28 are valid.

1.4 – Remote Fault

Bit 1.4 will be set to “1” if the Link Partner signals a far-end fault. The bit is cleared automatically upon a read if the far-end fault condition has been removed.

1.3 – Auto-Negotiation Capability

The VSC8211 is Auto-Negotiation capable, so this bit is hard-wired to “1”. Note that this bit will read a “1” even if Auto-Negotiation is disabled via bit 0.12.

1.2 – Link Status

This bit will return a “1” when the VSC8211 link state machine has reached the “link pass” state, meaning that a valid link has been established. If the link is subsequently lost, the Link Status will revert to a “0” state. It will remain a “0” until Link Status is read while the link state machine is in the “link pass” state.

1.1 – Jabber Detect

Note that Jabber Detect is required for 10BASE-T mode only. Jabber Detect will be set to “1” when the jabber condition is detected. Jabber Detect will be cleared automatically when this register is read.

1.0 – Extended Capability

The VSC8211 has extended register capability, so this bit is hard-wired to “1”.

25.3.3 Register 2 (02h) – PHY Identifier Register #1 - Clause 28/37 View

	Register 2 (02h) – PHY Identifier Register #1 - Clause 28/37 View				
Bit	**Name**	**Access**	**States**	**Reset Value**	**Sticky**
15:0	Organizationally Unique Identifier	RO	OUI most significant bits (Vitesse OUI bits 3:18)	0000000000001111 or (000Fh)	

2.15:0 – PHY Identifier Register #1

Vitesse has been assigned an OUI from the IEEE of 0003F1h. Per IEEE requirements, only OUI bits 3 to 18 are used in this register.

25.3.4 Register 3 (03h) – PHY Identifier Register #2 - Clause 28/37 View

	Register 3 (03h) – PHY Identifier Register #2 - Clause 28/37 View				
Bit	**Name**	**Access**	**States**	**Reset Value**	**Sticky**
15:10	Organizationally Unique Identifier	RO	OUI least significant bits (Vitesse OUI bits 19:24)	110001	
9:4	Vendor Model Number	RO	Vendor’s model number (IC)	001011 = VSC8211	
3:0	Vendor Revision Number	RO	Vendor’s revision number (IC)	0001 = Silicon Revision C	

3.15:10 – OUI

Vitesse has been assigned an OUI from the IEEE of 0003F1h. Per IEEE requirements, only OUI bits 19 to 24 are used in this register.

3.9:4 - Vendor Model Number

The Model no. of this IC is ‘001011’.

3.3:0 - Vendor Revision Number

The current Revision Number of this IC is ‘0001’.

25.3.5 Register 4 (04h) – Auto-Negotiation Advertisement Register

25.3.5.1 Clause 28 View

Register 4 (04h) – Auto-Negotiation Advertisement Register - Clause 28 View					
Bit	**Name**	**Access**	**States**	**Reset Value**	**Sticky**
15	Next-Page Transmission Request	R/W	1 = Next-Page transmission request	0	
14	Reserved	RO		0	
13	Transmit Remote Fault	R/W	1 = Transmit remote fault	0	
12	Reserved	RO		0	
11	Advertise Asymmetric Pause	R/W	1 = Advertise Asymmetric Pause capable	CMODE	
10	Advertise Symmetric Pause	R/W	1 = Advertise Symmetric Pause capable	CMODE	
9	Advertise 100BASE-T4 Capability	R/W	1 = 100BASE-T4 capable	0	
8	Advertise 100BASE-TX FDX	R/W	1 = 100BASE-TX FDX capable	CMODE	
7	Advertise 100BASE-TX HDX	R/W	1 = 100BASE-TX HDX capable	CMODE	
6	Advertise 10BASE-T FDX	R/W	1 = 10BASE-T FDX capable	CMODE	
5	Advertise 10BASE-T HDX	R/W	1 = 10BASE-T HDX capable	CMODE	
4:0	Advertise Selector Field	R/W		00001	

This register controls the advertised abilities of the local (not remote) PHY. The state of this register is latched when the Auto-Negotiation state machine enters the ABILITY_DETECT state. Thus, any writes to this register prior to completion of Auto-Negotiation as indicated by MII Register bit 1.5 should be followed by a re-negotiation for the new values to be properly used for Auto-Negotiation. Once Auto-Negotiation has completed, this register value may be read via the SMI to determine the highest common denominator technology.

4.15 – Auto-Negotiation Additional Next-Page Transmission Request

The VSC8211 supports additional Next-Page transmission through MII Register bit 4.15. See description of MII Register bit 18.1 for more details on Next-Page exchanges. This bit is only supported on copper media.

4.14, 4.12 – Reserved

4.13 – Transmit Remote Fault

This bit is used by the local MAC to communicate a fault condition to the link partner during auto-negotiation. This bit does not have any effect on the local PHY operation. This bit is automatically cleared following a successful negotiation with the Link Partner. Note that IEEE Clause-37 provides for two remote fault bits, while Clause-28 provides only a single remote fault bit. This discrepancy is handled in MII Extended Register bits 16E.2:1 - Remote Fault Mapping Mask and 16E.0 - Remote Fault Mapping OR.

4.11 – Advertise Asymmetric Pause Capability

This bit is used by the local MAC to communicate Asymmetric Pause Capability to the link partner during auto-negotiation. This has no effect on PHY operation. Changing this bit in Clause-28 view will also change bit 4.8 in Clause-37 view.

4.10 – Advertise Symmetric Pause Capability

This bit is used by the local MAC to communicate Symmetric Pause Capability to the link partner during autonegotiation. This has no effect on PHY operation. Changing this bit in Clause-28 view will also change bit 4.9 in Clause-37 view.

4.9:5 – Advertise Capability

Bits 4.9:5 allow the user to customize the ability information transmitted to the Link Partner during auto-negotiation. By writing a "1" to any of these bits, the corresponding ability will be advertised to the Link Partner. Writing a "0" to any bit causes the corresponding ability to be suppressed from transmission. The state of these bits has no other effect on the operation of the local PHY. Resetting the chip restores the default bit values. Note that the default values of these bits indicate the true ability of the VSC8211. These bits are not available for read or write in Clause-37 view, but remain valid for CAT-5 copper media.

4.4:0 – Advertise Selector Field

Since the VSC8211 is a member of the 802.3 class of PHYs, the Advertise Selector Field defaults to "00001". These bits are R/W because the Ethernet standard requires them to be R/W. Changing the value of these bits has no effect on PHY operation.

25.3.5.2 Clause 37 View

Register 4 (04h) – Auto-Negotiation Advertisement Register - Clause 37 View

Bit	Name	Access	States	Reset Value	Sticky
15	Next-Page Transmission Request	R/W	1 = Next-Page transmission request	0	
14	Reserved	RO		0	
13:12	Transmit Remote Fault	R/W	Remote fault transmission to link partner	00	
11:9	Reserved	RO		000	
8	Advertise Asymmetric Pause	R/W	1 = Advertise Asymmetric Pause capable	CMODE	
7	Advertise Symmetric Pause	R/W	1 = Advertise Symmetric Pause capable	CMODE	
6	Advertise 1000BASE-X HDX	R/W	1 = 1000BASE-X FDX capable	1	
5	Advertise 1000BASE-X FDX	R/W	1 = 1000BASE-X HDX capable	1	
4:0	Reserved	RO		00000	

4.15 – Auto-Negotiation Additional Next-Page Transmission Request

With copper media, this bit functions identically to Clause-28 view. Note, however, that the VSC8211 does not support next-page transmission over fiber 1000BASE-X media.

4.14 - Reserved

4.13:12 - Transmit Remote Fault

These bits are used by the local MAC to communicate a fault condition to the link partner during auto-negotiation. These bits do not have any effect on the local PHY operation. These bits are automatically cleared following a successful negotiation with the link partner. Note that IEEE Clause-37 provides for two remote fault bits, while Clause-28 provides only a single remote fault bit. This discrepancy is handled in MII Extended Register bits 16E.2:1 - Remote Fault Mapping Mask and 16E.0 - Remote Fault Mapping OR

4.11:9 - Reserved

4.8 – Advertise Asymmetric Pause Capability

This bit is used by the local MAC to communicate Asymmetric Pause Capability to the link partner during auto-negotiation. This has no effect on PHY operation. Changing this bit in Clause-37 view will also change bit 4.11 in Clause-28 view.

4.7 – Advertise Symmetric Pause Capability

This bit is used by the local MAC to communicate Symmetric Pause Capability to the link partner during autonegotiation. This has no effect on PHY operation. Changing this bit in Clause-37 view will also change bit 4.10 in Clause-28 view.

4.6:5 - Advertise 1000BASE-X Capability

Bits 4.6:5 control the 1000BASE-X capability advertisement transmitted to the link partner for both fiber and copper media. Changing these bits in Clause-37 view will also change MII Register bits 9.9:8 in Clause-28 view.

4.4:0 - Reserved

25.3.6 Register 5 (05h) – Auto-Negotiation Link Partner Ability Register

25.3.6.3 Clause 28 View

Register 5 (05h) – Auto-Negotiation Link Partner Ability Register - Clause 28 View

Bit	Name	Access	States	Reset Value	Sticky
15	LP Next-Page Transmit Request	RO	1 = LP NP transmit request	0	
14	LP Acknowledge	RO	1 = LP acknowledge	0	
13	LP Remote Fault	RO	1 = LP remote fault	0	
12	Reserved	RO		0	
11	LP Asymmetric Pause Capability	RO	1 = LP Advertise Asymmetric Pause capable	0	
10	LP Symmetric Pause Capability	RO	1 = LP Advertise Symmetric Pause capable	0	
9	LP Advertise 100BASE-T4 Capability	RO	1 = LP Advertise 100BASE-T4 capable	0	
8	LP Advertise 100BASE-TX FDX	RO	1 = LP 100BASE-TX FDX capable	0	
7	LP Advertise 100BASE-TX HDX	RO	1 = LP 100BASE-TX HDX capable	0	
6	LP Advertise 10BASE-T FDX	RO	1 = LP 10BASE-T FDX capable	0	
5	LP Advertise 10BASE-T HDX	RO	1 = LP 10BASE-T HDX capable	0	
4:0	LP Advertise Selector Field	RO	LP Advertise Selector Field	00000	

5.15 – LP Next-Page Transmit Request

Bit 5.15 returns a “1” when the Link Partner implements the Next-Page function and has Next-Page information it wants to transmit. The state of this bit is valid when the Auto-Negotiation Complete bit (1.5) or the Page Received bit (6.1) is set, and the current media type is CAT-5 copper.

5.14 – LP Acknowledge

Bit 5.14 returns a “1” when the Link Partner signals that it has successfully received the Link Code Word from the local PHY. The local PHY uses this bit for proper Link Code Word exchange, as defined in Clause 28 of IEEE 802.3.

5.13 – LP Remote Fault

Bit 5.13 returns a “1” when the Link Partner signals that a remote fault (from its perspective) has occurred. The local PHY does not otherwise use this bit. Note that IEEE Clause-37 provides for two remote fault bits, while Clause-28 provides only a single remote fault bit. This difference is handled in Extended MII Register bits 16E.2:1 - Remote Fault Mapping Mask and 16E.0 - Remote Fault Mapping OR. The state of this bit is valid when the Auto-Negotiation Complete bit (1.5) is set.

5.12 – Reserved

5.11 – LP Asymmetric Pause Capability

The LP Asymmetric Pause Capability bit indicates whether the Link Partner has asymmetric pause capability. The state of this bit is valid when the Auto-Negotiation Complete bit (1.5) is set.

5.10 – LP Symmetric Pause Capability

The LP Symmetric Pause Capability bit indicates whether the Link Partner supports symmetric pause frame capability. This bit is used by the Link Partner’s MAC to communicate symmetric pause capability to the local MAC. It has no effect on PHY operation. The state of this bit is valid when the Auto-Negotiation Complete bit (1.5) is set.

5.9:5 – LP Advertise Capability

Bits 5.9:5 reflect the abilities of the Link Partner. A “1” on any of these bits indicates that the Link Partner advertises capability of performing the corresponding mode of operation. These bits are not available for read in Clause-37 view, but remain valid for CAT-5 copper media and can be viewed by switching to Clause-28 view.

5.4:0 – LP Advertise Selector Field

Bits 5.4:0 indicate the state of the Link Partner’s Selector Field. The local PHY does not otherwise use these bits.

25.3.6.4 Clause 37 View

Register 5(05h) – Auto-Negotiation Link Partner Ability Register - Clause 37 View

Bit	Name	Access	States	Reset Value	Sticky
15	LP Next-Page Transmit Request	RO	1 = LP next-page transmission request	0	
14	LP Acknowledge	RO	1 = LP acknowledge	0	
13:12	LP Remote Fault	RO	LP remote fault	00	
11:9	Reserved	RO		000	
8	LP Advertise Asymmetric Pause	RO	1 = LP Advertise Asymmetric Pause	0	
7	LP Advertise Symmetric Pause	RO	1 = LP Advertise Symmetric Pause	0	
6	LP Advertise 1000BASE-X HDX	RO	1 = 1000BASE-X HDX capable	0	
5	LP Advertise 1000BASE-X FDX	RO	1 = 1000BASE-X FDX capable	0	
4:0	Reserved	RO		00000	

5.15 – LP Next-Page Transmit Request

In Clause-37 view, bit 5.15 functions identically to bit 5.15 in Clause-28 view.

5.14 - LP Acknowledge

In Clause-37 view, bit 5.14 functions identically to bit 5.14 in Clause-28 view.

5.13:12 – LP Remote Fault

Bits 5.13:12 return a “1” when the Link Partner signals that a remote fault (from its perspective) has occurred. The local PHY does not otherwise use these bits. Note that IEEE Clause-37 provides for two remote fault bits, while Clause-28 provides only a single remote fault bit. This discrepancy is handled in Extended MII Register bits 16E.2:1 - Remote Fault Mapping Mask and 16E.0 - Remote Fault Mapping OR . The state of this bit is valid when the Auto-Negotiation Complete bit (1.5) is set.

5.11:9 - Reserved

5.8 - LP Advertise Asymmetric Pause

In Clause-37 view, bit 5.8 functions identically to bit 5.11 in Clause-28 view. The state of this bit is valid when the Auto-Negotiation Complete bit (1.5) is set.

5.7 - LP Advertise Symmetric Pause

In Clause-37 view, bit 5.7 functions identically to bit 5.10 in Clause-28 view.The state of this bit is valid when the Auto-Negotiation Complete bit (1.5) is set.

5.6:5 - LP Advertise 1000BASE-X

Bits 5.6:5 reflect the 1000Mbit capability advertisement received from the link partner for both fiber and copper media. Therefore, these bits are set either if bits 5.6:5 are set during Clause-37 autonegotiation, or if MII Register bits 10.11:10 are set during Clause-28 autonegotiation.

5.4:0 - Reserved

25.3.7 Register 6 (06h) – Auto-Negotiation Expansion Register

25.3.7.5 Clause 28 View

Register 6 (06h) – Auto-Negotiation Expansion Register - Clause 28 View

Bit	Name	Access	States	Reset Value	Sticky
15:5	Reserved	RO		00000000000	
4	Parallel Detection Fault	RO LH	1 = Parallel detection fault	0	
3	LP Next-Page Able	RO	1 = LP Next-Page capable	0	
2	Local PHY Next-Page Able	RO	1 = Next-Page capable	1	
1	Page Received	RO LH	1 = New page has been received	0	
0	LP Auto-Negotiation Able	RO	1 = LP Auto-Negotiation capable	0	

6.15:5 – Reserved

6.4 – Parallel Detection Fault

Parallel Detection Fault returns a “1” when a parallel detection fault occurs in the local Auto-Negotiation state machine. Once set, this bit is automatically cleared when (and only when) Register 6 is read.

6.3 – LP Next-Page Able[1]

LP Next-Page Able returns a “1” when the Link Partner has Next-Page capabilities. This bit is used in the Auto-Negotiation state machines, as defined in Clause 28 of IEEE 802.3. The state of this bit is valid when either the Auto-Negotiation Complete bit (1.5) or the Page Received bit (6.1) is set.

6.2 – Local PHY Next-Page Able

Since the VSC8211 is next-page capable during Clause-28 autonegotiation, this bit is hard-wired to “1”.

6.1 – Page Received

Page Received is set to “1” when a new Link Code Word is received from the Link Partner, validated, and acknowledged. Page Received is automatically cleared when (and only when) Register 6 is read via the SMI.

6.0 – LP Auto-Negotiation Able[2]

LP Auto-Negotiation Capable is set to “1” if the Link Partner advertises Auto-Negotiation capability. The state of this bit is valid when the Auto-Negotiation Complete bit (1.5) or the Page Received bit (6.1) is set.

25.3.7.6 Clause 37 View

Register 6 (06h) – Auto-Negotiation Expansion Register - Clause 37 View

Bit	Name	Access	States	Reset Value	Sticky
15:3	Reserved	RO		0000000000000	
2	Local PHY Next-Page Able	RO	1 = Next-Page capable	0	
1	Page Received	RO LH	1 = New page has been received	0	
0	Reserved	RO		0	

[1]The state of this bit is valid only when the CAT5 media link is up.

[2]The state of this bit is vaild only when the CAT5 media link is up.

6.15:3 – Reserved

6.2 – Local PHY Next-Page Able

The VSC8211 is not next-page capable in Clause-37 auto-negotiation, therefore this bit is hard-wired to “0”. Note that this does not apply to bit 6.2 in Clause-28 auto-negotiation.

6.1 - Page Received

In Clause-37 view, bit 6.1 functions identically to bit 6.1 in Clause-28 view. Note, however, that next-pages can only be received by the VSC8211 during Clause-28 autonegotiation.

6.0 - Reserved

25.3.8 Register 7 (07h) – Auto-Negotiation Next-Page Transmit Register - Clause 28/37 View[1]

Register 7 (07h) – Auto-Negotiation Next-Page Transmit Register - Clause 28/37 View

Bit	Name	Access	States	Reset Value	Sticky
15	Next Page	R/W	1 = More pages follow 0 = Last page	0	
14	Reserved	RO		0	
13	Message Page	R/W	1 = Message page 0 = Unformatted page	1	
12	Acknowledge2	R/W	1 = Will comply with request 0 = Cannot comply with request	0	
11	Toggle	RO	1 = Previous transmitted LCW == 0 0 = Previous transmitted LCW == 1	0	
10:0	Message/Unformatted Code	R/W		00000000001	

7.15 – Next Page

The Next Page bit indicates whether this is the last Next-Page to be transmitted. By default, this bit is set to “0”, indicating that this is the last page.

7.14 – Reserved

7.13 – Message Page

The Message Page bit indicates whether this page is a message page or an unformatted page. This bit does not otherwise affect the operation of the local PHY. By default, this bit is set to “1”, indicating that this is a message page.

7.12 – Acknowledge2

The Acknowledge2 bit indicates if the local MAC reports that it is able to act on the information (or perform the task) indicated in the previous message. The local PHY does not interpret or act on changes in the state of this bit.

7.11 – Toggle

The Toggle bit is used by the arbitration function in the local PHY to ensure synchronization with the Link Partner during Next-Page exchanges. The Toggle bit is automatically set to the opposite state of the Toggle bit in the previously exchanged Link Code Word.

7.10:0 – Message/Unformatted Code

[1]This register is only valid for CAT-5 copper media

The Message/Unformatted Code bits indicate the message code being transmitted to the Link Partner. The local PHY passes the message code to the Link Partner without interpreting or reacting to it. By default, this code is set to “000 0000 0001”, indicating a null message.

25.3.9 Register 8 (08h)–Auto-Negotiation Link Partner Next-Page Receive Register,Clause 28/37 View[1]

Register 8 (08h) – Auto-Negotiation Link Partner Next-Page Receive Register - Clause 28/37 View					
Bit	**Name**	**Access**	**States**	**Reset Value**	**Sticky**
15	LP Next Page	RO	1 = More pages follow 0 = Last page	0	
14	LP Acknowledge	RO	1 = LP acknowledge	0	
13	LP Message Page	RO	1 = Message page 0 = Unformatted page	0	
12	LP Acknowledge2	RO	1 = LP will comply with request	0	
11	LP Toggle	RO	1 = Previous transmitted LCW == 0 0 = Previous transmitted LCW == 1	0	
10:0	LP Message/Unformatted Code	RO		00000000000	

SMI Register 8 contains the Link Partner’s Next-Page register contents. The contents of this register are only valid when the Page Received bit (6.1) is set.

8.15 – LP Next Page

This bit indicates if more pages follow from the Link Partner.

8.14 – LP Acknowledge

This bit returns a “1” when the Link Partner signals that it has received the Link Code Word from the local PHY. The local PHY uses this bit for proper Link Code Word exchange, as defined in Clause 28 of IEEE 802.3.

8.13 – LP Message Page

The Message Page bit indicates if the page received from the Link Partner is a message page or an unformatted page.

8.12 – LP Acknowledge2

The Acknowledge2 bit indicates whether the Link Partner MAC reports that it is able to act on the information (or perform the task) indicated in the message. The local PHY does not interpret or act on changes in the state of this bit.

8.11 – LP Toggle

The Toggle bit is used by the arbitration function in the local PHY to ensure synchronization with the Link Partner during Next-Page exchanges. In the Link Partner, the Toggle bit is automatically set to the opposite state of the Toggle bit in the previously exchanged Link Code Word from the Link Partner.

8.10:0 – LP Message/Unformatted Code

The Message/Unformatted Code bits indicate the message code being transmitted by the Link Partner.

[1]This register is only valid for CAT-5 copper media

25.3.10 Register 9 (09h) – 1000BASE-T Control Register

25.3.10.7 Clause 28 View[1]

Register 9 (09h) – 1000BASE-T Control Register - Clause 28 View					
Bit	**Name**	**Access**	**States**	**Reset Value**	**Sticky**
15:13	Transmitter Test Mode	R/W	Described below, per IEEE 802.3, 40.6.1.1.2	000	
12	MASTER/SLAVE Manual Configuration Enable	R/W	1 = Enable MASTER/SLAVE Manual Configuration value 0 = Disable MASTER/SLAVE Manual Configuration value	0	
11	MASTER/SLAVE Manual Configuration Value	R/W	1 = Configure PHY as MASTER during MASTER/SLAVE negotiation, only when bit 9.12 is set to logical one. 0 = Configure PHY as SLAVE during MASTER/SLAVE negotiation, only when bit 9.12 is set to logical one.	0	
10	Port Type	R/W	1 = Multi-port device 0 = Single-port device	0	
9	1000BASE-T FDX Capability	R/W	1 = PHY is 1000BASE-T FDX capable	CMODE	
8	1000BASE-T HDX Capability	R/W	1 = PHY is 1000BASE-T HDX capable	CMODE	
7:0	Reserved	R/W		00000000	

9.15:13 Transmitter/Receiver Test Mode[1]

This test is valid only in 1000BASE-T mode. Refer to IEEE 802.3-2002, section 40.6.1.1.2 for more information.

Bit 1 (9.15)	Bit 2 (9.14)	Bit 3 (9.13)	Test Mode
0	0	0	Normal operation
0	0	1	Test Mode 1 – Transmit waveform test
0	1	0	Test Mode 2 – Transmit jitter test in MASTER mode
0	1	1	Test Mode 3 – Transmit jitter test in SLAVE mode
1	0	0	Test Mode 4 – Transmitter distortion test
1	0	1	Reserved; operation not defined
1	1	0	Reserved; operation not defined
1	1	1	Reserved; operation not defined

- **Test Mode 1:** The PHY repeatedly transmits the following sequence of data symbols from all four transmitters: {{"+2" followed by 127 "0" symbols}, {"-2" followed by 127 "0" symbols}, {"+1" followed by 127 "0" symbols}, {"-1" followed by 127 "0" symbols}, {128 "+2" symbols, 128 "-2" symbols, 128 "+2" symbols, 128 "-2" symbols}, {1024 "0" symbols}}. The transmitter should use a 125.00 MHz ± 0.01% clock and should operate in MASTER timing mode.
- **Test Mode 2:** The PHY transmits the data symbol sequence {+2, -2} repeatedly on all channels. The transmitter should use a 125.00 MHz ± 0.01% clock in the MASTER timing mode.

[1]The state of this register is internally latched when the Auto-Negotiation state machine enters the ABILITY_DETECT state. Changes to the states of these bits are recognized only at that time. This register is valid only in 1000BASE-T mode.

- **Test Mode 3:** The PHY transmits the data symbol sequence {+2, -2} repeatedly on all channels. The transmitter should use a 125.00 MHz ± 0.01% clock and should operate in SLAVE timing mode.
- **Test Mode 4:** The PHY transmits the sequence of symbols generated by the following scrambler generator polynomial, bit generation, and level mappings:

  The maximum-length shift register used to generate the sequences defined by this polynomial is updated once per symbol interval (8ns). The bits stored in the shift register delay line at a particular time *n* are denoted by Scrn[10:0]. At each symbol period, the shift register is advanced by one bit, and one new bit represented by Scrn[0] is generated. Bits $Scr_n[8]$ and $Scr_n[10]$ are exclusive-OR'd together to generate the next $Scr_n[0]$ bit. The bit sequences, $x0_n$, $x1_n$, and $x2_n$, generated from combinations of the scrambler bits as shown in the following equations, shall be used to generate the quinary symbols, s_n, as shown in the following table. The transmitter should use a 125.00 MHz ± 0.01% clock and should operate in MASTER timing mode.

Table 35. Bit Sequences for Generating Quinary Symbols

$x2_n$	$x1_n$	$x0_n$	Quinary Symbol, s_n
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	-1
1	0	0	0
1	0	1	1
1	1	0	-2
1	1	1	-1

9.12 – MASTER/SLAVE Manual Configuration Enable[1]

When this bit is set to “0” (default), the MASTER/SLAVE designation of the local PHY is determined using the arbitration protocol established in the IEEE Ethernet standard. When this bit is set to “1”, the MASTER/SLAVE designation of the local PHY is set by bit 9.11. Note that MASTER/SLAVE configuration is valid only in 1000BASE-T mode.

9.11 – MASTER/SLAVE Configuration Value[1]

This bit is ignored when bit 9.12 is set to “0”. However, if bit 9.12 is set to “1”, bit 9.11 determines the MASTER/SLAVE designation of the local PHY. If bit 9.12 is set to “1” and bit 9.11 set to “0”, the local PHY is forced to be a SLAVE. If bit 9.12 is set to “1” and bit 9.11 set to “1”, the local PHY is forced to be a MASTER. Note that MASTER/SLAVE configuration is valid only in 1000BASE-T mode.

9.10 – Port Type[1]

Since the VSC8211 is a single port physical layer transceiver, bit 9.10 is set to “0” by default. When set to “0”, this bit indicates a preference for operation as a SLAVE. If the Link Partner does not indicate the same preference, the local PHY will operate as a SLAVE, and the Link Partner will be a MASTER. Otherwise, the normal MASTER/SLAVE assignment protocol is used.

9.9 – 1000BASE-T FDX[1]

Since the VSC8211 is 1000BASE-T FDX capable, this bit is “1” by default. If bit 9.9 is written to be “0”, the Auto-Negotiation state machine for the local PHY will be blocked from advertising 1000BASE-T FDX. Note that the Link Partner will be notified of

[1]The state of this register is internally latched when the Auto-Negotiation state machine enters the ABILITY_DETECT state. Changes to the states of these bits are recognized only at that time. This register is valid only in 1000BASE-T mode.

the state of 9.9 during Auto-Negotiation. After Auto-Negotiation is complete, changing the state of this bit has no effect unless Auto-Negotiation is manually restarted.

9.8 – 1000BASE-T HDX[1]

Since the VSC8211 is 1000BASE-T HDX capable, this bit is “1” by default. If bit 9.8 is written to be “0”, the Auto-Negotiation state machine for the local PHY will be blocked from advertising 1000BASE-T HDX. Note that the Link Partner will be notified of the state of bit 9.8 during Auto-Negotiation. After Auto-Negotiation is complete, changing the state of this bit has no effect unless Auto-Negotiation is manually restarted.

9.7:0 – Reserved

25.3.10.8 Clause 37 View

Register 9 (09h) - 1000BASE-T Control Register - Clause 37 View

Bit	Name	Access	States	Reset Value	Sticky
15:0	Reserved	RO		00000000 00000000	

9.15:0 - Reserved

In Clause-37 register view, MII register 9 is reserved. Note that MII register 9 bits in Clause-28 view remain valid, but cannot be read or written to if the current register view is Clause-37.

25.3.11 Register 10 (0Ah) – 1000BASE-T Status Register #1

25.3.11.9 Clause 28 View[2]

Register 10 (0Ah) – 1000BASE-T Status Register #1 - Clause 28 View

Bit	Name	Access	States	Reset Value	Sticky
15	MASTER/SLAVE Configuration Fault	RO LH SC	1 = MASTER/SLAVE configuration fault detected 0 = No MASTER/SLAVE configuration fault detected	0	
14	MASTER/SLAVE Configuration Resolution	RO	1 = Local PHY configuration resolved to MASTER 0 = Local PHY configuration resolved to SLAVE	1	
13	Local Receiver Status	RO	1 = Local receiver OK (loc_rcvr_status == OK) 0 = Local receiver not OK (loc_rcvr_status == NOT_OK)	0	
12	Remote Receiver Status	RO	1 = Remote receiver OK (rem_rcvr_status == OK) 0 = Remote receiver not OK (rem_rcvr_status == NOT_OK)	0	
11	LP 1000BASE-T FDX Capability	RO	1 = LP 1000BASE-T FDX capable 0 = LP not 1000BASE-T FDX capable	0	
10	LP 1000BASE-T HDX Capability	RO	1 = LP is 1000BASE-T HDX capable 0 = LP is not 1000BASE-T HDX capable	0	
9:8	Reserved	RO		00	
7:0	Idle Error Count	RO SC		00000000	

[1]The state of this register is internally latched when the Auto-Negotiation state machine enters the ABILITY_DETECT state. Changes to the states of these bits are recognized only at that time. This register is valid only in 1000BASE-T mode.

10.15 – MASTER/SLAVE Configuration Fault[1]

This bit indicates whether a MASTER/SLAVE configuration fault has been detected by the local PHY. A configuration fault occurs if both the local and remote PHYs are forced to the same MASTER/SLAVE state, or if no resolution is reached after seven retries. When such a fault has been detected, this bit is set to “1”, but the PHY continues to renegotiate until the MASTER/SLAVE configuration is resolved. Once set, this bit is automatically cleared when (and only when) Register 10 is read via the SMI.

10.14 – MASTER/SLAVE Configuration Resolution[1]

By default, the MASTER/SLAVE configuration is determined as part of the Auto-Negotiation process. However, the MASTER/SLAVE status can optionally be manually forced via bits in MII Register 9. Bit 10.14 indicates the final MASTER/SLAVE configuration status for the local PHY. This bit can change state only as a result of the reset or subsequent restart of the Auto-Negotiation process. This bit is only valid when the Auto-Negotiation Complete bit (1.5) is set.

10.13 – Local Receiver Status[1]

Bit 10.13 indicates the state of the loc_rcvr_status flag within the PMA receive function within the local PHY.

10.12 – Remote Receiver Status[1]

Bit 10.12 indicates the state of the rem_rcvr_status flag within the PMA receive function within the local PHY.

10.11 – LP 1000BASE-T FDX Capability[1, 3]

Bit 10.11 is set to “1” if the Link Partner PHY advertises 1000BASE-T FDX capability. Otherwise, this bit is set to “0”. This bit is valid on when MII Register 1.5 is set.

10.10 – LP 1000BASE-T HDX Capability[2, 3]

Bit 10.10 is set to “1” if the Link Partner PHY advertises 1000BASE-T HDX capability. Otherwise, this bit is set to “0”. This bit is valid on when MII Register 1.5 is set.

10.9:8 – Reserved

10.7:0 – Idle Error Count[3]

Bits 10.7:0 indicate the Idle Error count, where 10.7 is the most significant bit. These bits contain a cumulative count of the errors detected when the receiver is receiving idles and PMA_TXMODE.indicate is equal to SEND_N (indicating that both the local and remote receiver status have been detected to be OK). The counter is incremented every symbol period that rx_error_status in the PMA receive function is equal to ERROR. Bits 10.7:0 are reset to all “0”s when the error count is read by the management function, or upon execution of the PCS reset function, and they are saturated to all “1”s in case of overflow.

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[2]The bits in this register apply only in 1000BASE-T mode.

[1]This bit is valid only when the Page Received bit (6.1) is set to a “1”.

[2]This bit applies only in 1000BASE-T mode.

[3]The state of this bit is valid only if MII Register 9.9 or 9.8 is set.

25.3.11.10 Clause 37 View

Register 10 (0Ah) - 1000BASE-T Status Register #1 - Clause 37 View					
Bit	**Name**	**Access**	**States**	**Reset Value**	**Sticky**
15:0	Reserved	RO		00000000 00000000	

9.15:0 - Reserved

In Clause-37 register view, MII register 10 is reserved. Note that MII register 10 bits in Clause-28 view remain valid, but cannot be read if the current register view is Clause-37.

25.3.12 Register 11 (0Bh) – Reserved Register

Register 11 (0Bh) – Reserved Register					
Bit	**Name**	**Access**	**States**	**Reset Value**	**Sticky**
15:0	Reserved	RO		00000000 00000000	

11.15:0 – Reserved

25.3.13 Register 12 (0Ch) – Reserved Register

Register 12 (0Ch) – Reserved Register					
Bit	**Name**	**Access**	**States**	**Reset Value**	**Sticky**
15:0	Reserved	RO		00000000 00000000	

12.15:0 – Reserved

25.3.14 Register 13 (0Dh) – Reserved Register

Register 13 (0Dh) – Reserved Register					
Bit	**Name**	**Access**	**States**	**Reset Value**	**Sticky**
15:0	Reserved	RO		00000000 00000000	

13.15:0 – Reserved

25.3.15 Register 14 (0Eh) – Reserved Register

Register 14 (0Eh) – Reserved Register					
Bit	**Name**	**Access**	**States**	**Reset Value**	**Sticky**
15:0	Reserved	RO		00000000 00000000	

14.15:0 – Reserved

25.3.16 Register 15 (0Fh) – 1000BASE-T Status Register #2

25.3.16.11 Clause 28 View

Register 15 (0Fh) – 1000BASE-T Status Register #2 - Clause 28 View

Bit	Name	Access	States	Reset Value	Sticky
15	1000BASE-X FDX Capability	RO	1 = PHY is 1000BASE-X FDX capable 0 = PHY is not 1000BASE-X FDX capable	0	
14	1000BASE-X HDX Capability	RO	1 = PHY is 1000BASE-X HDX capable 0 = PHY is not 1000BASE-X HDX capable	0	
13	1000BASE-T FDX Capability	RO	1 = PHY is 1000BASE-T FDX capable 0 = PHY is not 1000BASE-T FDX capable	1	
12	1000BASE-T HDX Capability	RO	1 = PHY is 1000BASE-T HDX capable 0 = PHY is not 1000BASE-T HDX capable	1	
11:0	Reserved	RO		000000000000	

15.15 – 1000BASE-X FDX Capability

The VSC8211 is not 1000BASE-X capable, so this bit is hard-wired to “0”.

15.14 – 1000BASE-X HDX Capability

The VSC8211 is not 1000BASE-X capable, so this bit is hard-wired to “0”.

15.13 – 1000BASE-T FDX Capability

The VSC8211 is 1000BASE-T FDX capable, so this bit is hard-wired to “1”.

15.12 – 1000BASE-T HDX Capability

The VSC8211 is 1000BASE-T HDX capable, so this bit is hard-wired to “1”.

15.11:0 – Reserved

25.3.16.12 Clause 37 View

Register 15 (0Fh) – 1000BASE-T Status Register #2 - Clause 37 View

Bit	Name	Access	States	Reset Value	Sticky
15	1000BASE-X FDX Capability	RO	1 = PHY is 1000BASE-X FDX capable 0 = PHY is not 1000BASE-X FDX capable	1	
14	1000BASE-X HDX Capability	RO	1 = PHY is 1000BASE-X HDX capable 0 = PHY is not 1000BASE-X HDX capable	1	
13	1000BASE-T FDX Capability	RO	1 = PHY is 1000BASE-T FDX capable 0 = PHY is not 1000BASE-T FDX capable	0	
12	1000BASE-T HDX Capability	RO	1 = PHY is 1000BASE-T HDX capable 0 = PHY is not 1000BASE-T HDX capable	0	
11:0	Reserved	RO		000000000000	

15.15:12 – 1000BASE-X Capability

In Clause-37 view, bits 15.15:12 differ from bits 15.15:12 in Clause-28 view by their reset values only. In Clause 37 view MII Register 15.15:12 = '0011'.

15:11:0 - Reserved

25.3.17 Register 16 (10h) – Reserved

Register 16 (10h) – Reserved Register					
Bit	**Name**	**Access**	**States**	**Reset Value**	**Sticky**
15:0	Reserved	RO		00000000 00000000	

16.15:0 – Reserved

25.3.18 Register 17 (11h) – Reserved

Register 17 (11h) – Reserved Register					
Bit	**Name**	**Access**	**States**	**Reset Value**	**Sticky**
15:0	Reserved	RO		00000000 00000000	

17.15:0 – Reserved

25.3.19 Register 18 (12h) – Bypass Control Register

Register 18 (12h) – Bypass Control Register					
Bit	**Name**	**Access**	**States**	**Reset Value**	**Sticky**
15	Reserved	RO		0	
14	Bypass 4B5B Encoder/Decoder	R/W	1 = Bypass 4B5B encoder/decoder 0 = Enable 4B5B encoder/decoder	0	
13	Bypass Scrambler	R/W	1 = Bypass scrambler 0 = Enable scrambler	0	
12	Bypass Descrambler	R/W	1 = Bypass descrambler 0 = Enable descrambler	0	
11:9	Reserved	RO		000	
8	Transmitter Test Clock Enable	R/W	1 = Enable TXCLK test output on CLKOUTMI-CRO pin 0 = Disable TXCLK test output on CLKOUTMI-CRO pin	0	
7:6	Reserved	RO		00	
5	Disable Automatic Pair Swap Correction	R/W	1 = Disable 0 = Enable	0	
4	Disable Polarity Inversion	R/W	1 = Disable 0 = Enable	0	
3	Parallel-Detect Control	R/W	1 = Do not ignore advertised ability 0 = Ignore advertised ability	1	S
2	Reserved	RO		0	
1	Disable Automatic 1000BASE-T Next-Page Exchange	R/W	1 = Disable automatic 1000BASE-T Next-Page exchanges 0 = Enable automatic 1000BASE-T Next-Page exchanges	0	S
0	CLKOUTMAC Output Enable	R/W	1 = Enable output clock pins CLKOUTMAC 0 = Disable output clock pins CLKOUTMAC	1	S

18.15 – Reserved

18.14 – Bypass 4B5B Encoder/Decoder [1]

When bit 18.14 is set to “1”, the 5B codes (TXER and TXD[3:0]) will be passed from the MII interface directly to the scrambler, bypassing the 4B5B encoder. Note that in this mode, J/K and T/R code insertion will not be performed. The receiver will pass descrambled/aligned 5B codes directly to the MII interface (RXER and RXD[3:0]), bypassing the 4B5B decoder. Carrier sense (CRS) is still asserted when a valid frame is detected.

18.13 – Bypass Scrambler[2]

When bit 18.13 is set to “1”, the scrambler is disabled.

18.12 – Bypass Descrambler[2]

When bit 18.12 is set to “1”, the descrambler is disabled.

[1]This bit applies only in 100BASE-TX mode.
[2]This bit applies only in 100BASE-TX and 1000BASE-T modes.

18.11:9 – Reserved

18.8 – Transmitter Test Clock Enable

When a “1” is written to bit 18.8, the CLKOUTMICRO output pin becomes a test pin for the transmit clock “TXCLK”. This capability is intended to enable measurement of transmitter timing jitter, as specified in IEEE Standard 802.3-2002, section 40.6.1.2.5. When in IEEE-specified transmitter test modes 2 or 3 (see IEEE 802.3-2002, section 40.6.1.1.2 and MII Register bits 9.15:13), the peak-to-peak jitter of the zero-crossings of the differential signal output at the MDI, relative to the corresponding edge of TXCLK, is measured. The corresponding edge of TXCLK is the edge of the transmit test clock, in polarity and time, that generates the zero-crossing transition being measured.

While transmitter test mode clock TXCLK is intended only for characterization test purposes, CLKOUTMICRO is intended to serve as a general purpose system or MAC reference clock.

18.7:6 – Reserved

18.5 - Disable Automatic Pair Swap Correction

When set to “1”, the automatic pair swap correction feature of the PHY is disabled.

18.4 - Disable Polarity Inversion

When set to “1”, the automatic polarity inversion feature of the PHY is disabled.

18.3 – Parallel-Detect Control

When bit 18.3 is “1”, MII Register 4, bits [8:5], are taken into account when attempting to parallel-detect. This is the default behavior expected by the standard. Setting 18.3 to a “0” will result in Auto-Negotiation ignoring the advertised abilities, as specified in MII Register 4, during parallel detection of a non-auto-negotiating 10BASE-T or 100BASE-TX PHY.

18.2 – Reserved

18.1 – Disable Automatic 1000BASE-T Next-Page Exchanges

Bit 18.1 is used to control the automatic exchange of 1000BASE-T Next-Pages defined in IEEE 802.3-2002 (Annex 40C). When this bit is set, the automatic exchange of these pages is disabled, and the control is returned to the user through the SMI after the base page has been exchanged. The user then has complete responsibility to:

- send the correct sequence of Next-Pages to the Link Partner, *and*
- determine common capabilities and force the device into the correct configuration following successful exchange of pages.

When bit 18.1 is reset to “0”, the 1000BASE-T related Next-Pages are automatically exchanged without user intervention. If the Next Page bit 4.15 was set by the user in the Auto-Negotiation Advertisement register at the time the Auto-Negotiation was restarted, control is returned to the user for additional Next-Pages following the 1000BASE-T Next-Page exchange.

If both bit 18.1 and MII Register bit 4.15 are reset when an Auto-Negotiation sequence is initiated, all Next-Page exchange is automatic, including sourcing of null pages. No user notification is provided until either Auto-Negotiation completes or fails. See the description of MII Register bit 4.15 for more details on standard Next-Page exchanges.

18.0 – CLKOUTMAC Output Enable

When bit 18.0 is set to “1”, the VSC8211 provides a 125MHz clock on the CLKOUTMAC output pin. The electrical specification for this clock corresponds to the current settings for VDDIOMAC. This clock is for use by the MAC, system manager CPU, or control logic. By default, this pin is enabled, which enables the clock output independent of the status of any link, unless the hardware reset is active (which also powers down the PLL). When disabled, the clock pins are normally driven low.

25.3.20 Register 19 (13h) – Reserved

Register 19 (13h) – Reserved					
Bit	**Name**	**Access**	**States**	**Reset Value**	**Sticky**
15:0	Reserved	RO		00000000 00000000	

19.15:0 - Reserved

25.3.21 Register 20 (14h) – Reserved

Register 20 (14h) – Reserved					
Bit	**Name**	**Access**	**States**	**Reset Value**	**Sticky**
15:0	Reserved	RO		00000000 00000000	

20.15:0 – Reserved

25.3.22 Register 21 (15h) – Reserved

Register 21 (15h) – Reserved					
Bit	**Name**	**Access**	**States**	**Reset Value**	**Sticky**
15:0	Reserved	RO		00000000 00000000	

21.15:0 – Reserved

25.3.23 Register 22 (16h) – Control & Status Register

Register 22 (16h) – Control & Status Register					
Bit	**Name**	**Access**	**States**	**Reset Value**	**Sticky**
15	Disable Link Integrity State Machine	R/W	1 = Disable link integrity test 0 = Enable link integrity test	0	S
14	Disable jabber Detect	R/W	1 = Disable jabber detect 0 = Enable jabber detect	0	S
13	Disable 10BASE-T Echo	R/W	1 = Disable 10BASE-T Echo 0 = Enable 10BASE-T Echo	CMODE	S
12	SQE Disable Mode	R/W	1 = Disable SQE Transmit 0 = Enable SQQ Transmit	CMODE	S
11:10	10BASE-T Squelch Control	R/W	00 = Normal squelch 01 = Low squelch 10 = High squelch 11 = Reserved	00	S
9	Sticky Reset Enable	R/W	1 = All bits marked as sticky will retain their values during software reset 0 = All bits marked as sticky will be changed to default values during software reset	1	SS
8	EOF Error	RO SC	1 = EOF error detected since last read 0 = EOF error not detected since last read	0	
7	10BASE-T Disconnect State	RO SC	1 = 10BASE-T link disconnected 0 = 10BASE-T link connected	0	
6	10BASE-T Link Status	RO	1 = 10BASE-T link active 0 = 10BASE-T link inactive	0	
5:3	Reserved	RO		00	
2:1	CRS Control	R/W	See table in register description below	00	S
0	Reserved	RO		0	

22.15 – Disable Link-Integrity State Machine[1]

When bit 22.15 is set to “0”, the VSC8211 link integrity state machine runs automatically. When bit 22.15 is set to “1”, the link integrity state machine is bypassed, and the PHY is forced into link pass status.

22.14 – Disable Jabber Detect[1]

When bit 22.14 is set to “0”, the VSC8211 automatically shuts off the transmitter when a transmission request exceeds the IEEE-specified time limit. When bit 22.14 is set to “1”, transmission requests are allowed to be arbitrarily long without shutting down the transmitter.

22.13 – Disable 10BASE-T Echo Mode[1]

When this bit is set, TXEN and TXD will not be echoed on the RXDV abd RXD pins respectively in 10BASE-T half duplex mode.

22.12 – SQE Disable Mode[2]

When bit 22.12 is set to “1”, SQE (Signal Quality Error) pulses are not sent. Note that this control bit applies in 10BASE-T HDX mode only.

[1]This bit applies only in 10BASE-T mode.
[2]This bits applies only in 10BASE-T HDX mode.

22.11:10 – 10BASE-T Squelch Control[1]

When bits 22.11:10 are set to “00”, the VSC8211 uses the squelch threshold levels prescribed by the IEEE’s 10BASE-T specification. When bits 22.11:10 are set to “01”, the squelch level is decreased, which may improve the bit error rate performance on long loops. When bits 22.11:10 are set to “10”, the squelch level is increased, which may improve the bit error rate in high-noise environments.

22.9 - Sticky Reset Enable

When bit 22.9 is set, all MII register bits that are marked with an “S” in the “sticky” column will retain their values during a software reset. When cleared, all MII register bits that are marked with an “S” in the “sticky” column will be changed to their default values during a software reset. Note that bits marked with an “SS” retain their values across software reset regardless of the setting of bit 22.9.

22.8 – EOF Error[1]

When bit 22.8 returns a “1”, a defective EOF (End-of-Frame) sequence has been received since the last time this bit was read. This bit is automatically set to “0” when it is read.

22.7 – 10BASE-T Disconnect State

Bit 22.7 is set to “1” if the 10BASE-T connection has been broken by the carrier integrity monitor since the last read of this bit; otherwise, this bit is set to “0”.

22.6 – 10BASE-T Link Status

Bit 22.6 is set to “1” if the 10BASE-T link is active. Otherwise, this bit is set to “0”.

22.5:3 – Reserved

22.2:1 - CRS Control

Bits 22.2:1 determine the behavior of the CRS indication provided by the VSC8211 according to the following table:

		CRS Control Bits - bits 2:1			
		00 (default)	**01**	**10**	**11**
Link State	**1000BASE-T Full-Duplex**	CRS = RXDV	CRS = 0	CRS = RXDV	CRS = 0
	1000BASE-T Half-Duplex	CRS = Logical OR of RXDV and TXEN	CRS = Logical OR of RXDV and TXEN	CRS = RXDV	CRS = RXDV
	100BASE-TX Full-Duplex	CRS = RXDV	CRS = 0	CRS = RXDV	CRS = 0
	100BASE-TX Half-Duplex	CRS = Logical OR of RXDV and TXEN	CRS = Logical OR of RXDV and TXEN	CRS = RXDV	CRS = RXDV
	10BASE-T Full-Duplex	CRS = RXDV	CRS = 0	CRS = RXDV	CRS = 0
	10BASE-T Half-Duplex	CRS = Logical OR of RXDV and TXEN	CRS = Logical OR of RXDV and TXEN	CRS = RXDV	CRS = RXDV

22.0 – Reserved

[1]This bit applies only in 10BASE-T mode.

25.3.24 Register 23 (17h) – PHY Control Register #1

Register 23 (17h) – PHY Control Register #1					
Bit	**Name**	**Access**	**States**	**Reset Value**	**Sticky**
15:12	MAC/Media Interface Mode Select	RWSW	See Table 36 below	CMODE	
11:10	RGMII/RTBI TXC Skew Selection	R/W	00 = No skew on TXC 01 = 1.5ns skew on TXC 10 = 2.0ns skew on TXC 11 = 2.5ns skew on TXC	CMODE	S
9:8	RGMII/RTBI RXC Skew Selection	R/W	00 = No skew on RXC 01 = 1.5ns skew on RXC 10 = 2.0ns skew on RXC 11 = 2.5ns skew on RXC	CMODE	S
7	EWRAP Enable	R/W	1 = Enable EWRAP in TBI mode 0 = Disable EWRAP in TBI mode	0	
6	TBI Bit Order Reversal Enable	R/W	1 = Enable TBI bit order reversal 0 = Disable TBI bit order reversal	0	S
5	RX Idle Clock Enable	R/W	1 = 25MHz clock on RXCLK pin enabled in Enhanced ActiPHY mode 0 = 25MHz clock on RXCLK pin disabled in Enhanced ActiPHY mode	1	SS
4	Register View	RWSW	0 = MII registers 0:15 correspond to the definition in IEEE802.3 clause 28.2.4 (copper media) 1 = MII registers 0:15 correspond to the definition in IEEE802.3 clause 37.2.5 (fiber media)	CMODE	SS
3	Far End (Media-Side) Loopback Enable	R/W	1 = Far End (Media side) Loopback is enabled 0 = Far End (Media side) Loopback is disabled	0	
2:1	MAC/Media Interface Mode Select	RWSW	SeeTable 36 below	CMODE	
0	EEPROM Status	RO	1 = EEPROM is detected on EEPROM interface 0 = EEPROM is not detected on EEPROM interface	0	

23.15:12, 2:1– MAC/Media Interface Mode Select

Bits 23.15:12 and 23.2:1 are used to select the MAC interface modes and media interface modes. The reset value for these bits is dependent upon the state of the MAC Interface bits in the CMODE hardware configuration. All combinations of these bits not indicated below are reserved:

Table 36. PHY Operating Modes

Operating Mode Category	MII Register 23.15:12, 23.2:1	CMODE2 [3:0]	MAC Interface	Media Interface	Other Settings
Parallel MAC PHY Operating Modes	0011,10	1000	GMII/MII	CAT5	
	0011,01	0010	GMII	Fiber	
	0010,01	0011	GMII/MII	Auto Media Sense	Fiber Preference
	0010,10	-	GMII/MII	Auto Media Sense	CAT5 Preference[1]
	0001,10	0110	RGMII	CAT5	
	0001,01	0111	RGMII	Fiber	
	0000,01	0001	RGMII	Auto Media Sense	Fiber Preference
	0000,10	-	RGMII	Auto Media Sense	CAT5 Preference[1]
	0110,00	1001	TBI	CAT5	With Clause 37 Auto-Negotiation Detection
	0111,01	1011	TBI	Fiber[2]	
	0100,00	1100	RTBI	CAT5	With Clause 37 Auto-Negotiation Detection
	0101,01	-	RTBI	Fiber[2]	
Serial MAC PHY Operating Modes	1111,00	0100	802.3z SerDes	CAT5	Clause 37 disabled
	1110, 01	1110	802.3z SerDes	CAT5	Clause 37 enabled
	1110,10	1010	802.3z SerDes	CAT5	Clause 37 enabled, Media Convertor Mode
	1110,00	0000	802.3z SerDes	CAT5	With Clause 37 Auto-Negotiation Detection
	1010,01	1111	SGMII	CAT5	625Mhz SCLK Clock Disabled
	1000,01	0101	SGMII	CAT5	625MHz SCLK Clock Enabled
	1001,01	1101	Serial	Serial	Buffered Mode – With Clock Recovery[3]
	1001,00		SGMII	CAT5	Modified Clause 37 auto-negotiation disabled, 625MHz SCLK Clock Enabled
	1011,00		SGMII	CAT5	Modified Clause 37 auto-negotiation disabled, 625MHz SCLK Clock Disabled

[1] In this mode, the PHY does not drop the Fiber Media link if the CAT5 link comes up after the Fiber Link has been established. It is therefore not a suitable mode for unmanaged applications. For more information on how to use this mode in managed applications, contact your Vitesse representative.
[2] PHY registers are not supported in this mode.
[3] In this mode, the PHY's MAC and media interfaces are the same. Both interfaces can be either SGMII or 802.3z SerDes.

23.11:10 – RGMII/RTBI TXC Skew Selection

Bits 23.11:10 specify the amount of clock delay added to the TX_CLK line inside the VSC8211 when using an RGMII or RTBI interface. By enabling this internal delay, a PCB "trombone" delay is not required as specified by the RGMII standard. Multiple values are provided to compensate for PCB trace skews. The default values of these bits are specified by the RGMII Skew bits in the CMODE hardware configuration. See Table 27, "PHY Operating Condition Parameter Description," on page 68 for more information.

23.9:8 – RGMII/RTBI RXC Skew Selection

Bits 23.9:8 specify the amount of clock delay added to the RX_CLK line inside the VSC8211 when using an RGMII or RTBI interface. By enabling this internal delay, a PCB "trombone" delay is not required as specified by the RGMII standard. Multiple

values are provided to compensate for PCB trace skews. The default values of these bits are specified by the RGMII Skew bits in the CMODE hardware configuration. See Table 27, "PHY Operating Condition Parameter Description," on page 68 for more information.

23.7 – EWRAP Enable

When bit 23.7 is set to "1" and the MAC interface is set to TBI, data loopback is enabled on the MAC interface.

23.6 – TBI Bit Order Reversal Enable

Bit 23.6 allows the user to specify the bit order for the PCS when TBI mode is selected. By default, TBI bit order reversal, as defined in the IEEE standard, is disabled.

23.5 – RX Idle Clock Enable

When bit 23.5 is set to "1", a 25MHz clock is enabled on the RXCLK pin when the VSC8211 is in Enhanced ActiPHY mode. When bit 23.5 is cleared, the RXCLK pin remains low during Enhanced ActiPHY mode. This clock is enabled by default.

23.4 – Register View

When bit 23.4 is set to "1", MII registers 0:15 correspond to the definition in IEEE802.3 clause 28.2.4 (copper media). When bit 23.4 is cleared, MII registers 0:15 correspond to the definition in IEEE802.3 clause 37.2.5 (fiber media). Bit 23.4 is set to "1" by default. Refer to Section 25.1: "Clause 28/37 Resister View" on page 82 for more information.

23.3 – Far End (Media-Side) Loopback Enable[1]

When bit 23.3 is set to "1", all incoming data from the link partner on the current media interface is retransmitted back to the link partner on the media interface. In addition, the incoming data will also appear on the RX pins of the MAC interface. Any data present on the TX pins of the MAC interface is ignored by the VSC8211 when bit 23.3 is set. In order to avoid loss of data, bit 23.3 should not be set while the VSC8211 is receiving data on the media interface. Bit 23.3 applies to all operating modes of the VSC8211. When bit 23.3 is cleared, the VSC8211 resumes normal operation. This bit is cleared by default. Refer to section 18.3, "Far-end Loopback," page 64.

23.0 – EEPROM Status

When bit 23.0 is set to "1", an EEPROM has been detected on the external EEPROM interface. When cleared, bit 23.0 indicates that no EEPROM has been detected.

[1]This feature is not available in 'TBI to CAT5 Media' PHY operating mode.

25.3.25 Register 24 (18h) – PHY Control Register #2

Register 24 (18h) – PHY Control Register #2					
Bit	**Name**	**Access**	**States**	**Reset Value**	**Sticky**
15:13	Reserved[1]	RO		111	S
12	Enable PICMG Miser Mode[2]	R/W	1 = PICMG Miser Mode Enabled 0 = PICMG Miser Mode Disabled	0	S
11:10	Reserved	RO		00	
9:7	TX FIFO Depth Control for RGMII, SGMII and Serial MAC	R/W	000 to 010 = Reserved 011 = Jumbo packet mode 100 = IEEE mode 101 to 111 = Reserved	100	S
6:4	RX FIFO Depth Control (RTBI only)	R/W	000 to 010 = Reserved 011 = Jumbo packet mode 100 = IEEE mode 101 to 111 = Reserved	100	S
3:1	Reserved	RO		000	
0	Connector Loopback	R/W	1 = Active (See Section 18.5: "Connector Loopback" for details) 0 = Disable	0	

[1] These bits must always be written to as '111'.
[2] See section 12, "Transformerless Operation for PICMG 2.16 and 3.0 IP-based Backplanes," page 45 for more information.

24.15:13 – Reserved

These bits must always be written to as '111'.

24.12 - Enable PICMG Miser Mode[1]

Setting bit 24.12 turns off some portions of the PHY's DSP block and reduces the PHY's Operating power. This bit can be set in order to reduce power consumption in applications where the signal to noise ratio on the CAT-5 media is high, such as ethernet over the backplane or where the cable length is short (<10m).

24.11:10 - Reserved

24.9:7 – TX FIFO Depth Control for RGMII, SGMII and Serial MAC[2]

Bits 24.9:7 control symbol buffering for the transmit synchronization FIFO used in all 1000BT modes except for RTBI-Serdes/ Fiber mode. An internal FIFO is used to synchronize the clock domains between the MAC transmit clock and the PHY's clock (e.g., REFCLK), used to transmit symbols on the local PHY's twisted pair interface.

The IEEE mode supports up to 1518-byte packet size with the minimum inter-packet gap (IPG). The jumbo packet mode adds latency to the path to support up to 9600-byte packets with the minimum inter-packet gap (IPG). When using jumbo packet mode, a larger IPG is recommended due to the possible compression of the IPG at the output of the FIFO.

[1]See section 12, "Transformerless Operation for PICMG 2.16 and 3.0 IP-based Backplanes," page 45 for more information.
[2]The TX and RX FIFOs are not used in MII mode for 10BASE-T and 100BASE-TX.

24.6:4 – RX FIFO Depth Control[1]

Used in 1000BT Serial MAC, SGMII, and RTBI modes only, bits 24.6:4 control symbol buffering as determined by the receive synchronization FIFO. An internal FIFO is used to synchronize the clock domains between the MAC receive clock and the PHY's clock (e.g., REFCLK), used to receive symbols on the local PHY's twisted pair interface.

The IEEE mode supports up to 1518-byte packet size with the minimum inter-packet gap (IPG). The jumbo packet mode adds latency to the path to support up to 9600-byte packets with the minimum inter-packet gap (IPG). When using jumbo packet mode, a larger IPG is recommended due to the possible compression of the IPG at the output of the FIFO.

24.3:1 – Reserved

24.0 - Connector Loopback[2]

See Section 18.5: "Connector Loopback" for details.

[1]The TX and RX FIFOs are not used in MII mode for 10BASE-T and 100BASE-TX.

[2]MII Register bit 18.5 must also be set to enable this feature.

25.3.26 Register 25 (19h) – Interrupt Mask Register

Register 25 (19h) – Interrupt Mask Register					
Bit	**Name**	**Access**	**States**	**Reset Value**	**Sticky**
15	Interrupt Pin Enable	R/W	1 = Enable interrupt pin 0 = Disable interrupt pin	0	S
14	Reserved	RO		0	
13	Link State-Change	R/W	1 = Enable Link State interrupt 0 = Disable Link State interrupt	0	S
12	Reserved	RO		0	
11	Auto-Negotiation Error Interrupt Mask	R/W	1 = Enable Auto-Negotiation Error interrupt 0 = Disable Auto-Negotiation Error interrupt	0	S
10	Auto-Negotiation-Done / Interlock Done Interrupt Mask	R/W	1 = Enable Auto-Negotiation-Done/ Interlock Done interrupt 0 = Disable Auto-Negotiation-Done/ Interlock Done interrupt	0	S
9	Inline Powered Device Detected Interrupt Mask	R/W	1 = Enable Inline Powered Device Detected interrupt 0 = Disable Inline Powered Device Detected interrupt	0	S
8	Symbol Error Interrupt Mask	R/W	1 = Enable Symbol Error interrupt 0 = Disable Symbol Error interrupt	0	S
7	Descrambler Lock-Lost Interrupt Mask	R/W	1 = Enable Lock-Lost interrupt 0 = Disable Lock-Lost interrupt	0	S
6	TX FIFO Interrupt Mask	R/W	1 = Enable TX FIFO interrupt 0 = Disable TX FIFO interrupt	0	S
5	RX FIFO Interrupt Mask	R/W	1 = Enable RX FIFO interrupt 0 = Disable RX FIFO interrupt	0	S
4	AMS Media Change Interrupt Mask	R/W	1 = Enable AMS Media Change interrupt 0 = Disable AMS Media Change interrupt	0	S
3	False Carrier Interrupt Mask	R/W	1 = Enable False Carrier interrupt 0 = Disable False Carrier interrupt	0	S
2	Cable Impairment Detect Interrupt Mask	R/W	1 = Enable Cable Impairment Detect interrupt 0 = Disable Cable Impairment Detect interrupt	0	S
1	MASTER/SLAVE Resolution Error Interrupt Mask	R/W	1 = Enable MASTER/SLAVE interrupt 0 = Disable MASTER/SLAVE interrupt	0	S
0	RXER Interrupt	R/W	1 = Enable RX_ER interrupt 0 = Disable RX_ER interrupt	0	S

25.15 – Interrupt Pin Enable

When bit 25.15 is set to “1”, the hardware interrupt is enabled, meaning that the state of the external interrupt pin (MDINT) can be influenced by the state of the Interrupt Status bit (26.15). When bit 25.15 is set to “0”, the interrupt status bits (MII Register 26) continue to be set in response to interrupts, but the interrupt hardware pin MDINT on the VSC8211 will not be influenced.

25.14 – Reserved

25.13 – Link State-Change Interrupt Mask

When bit 25.13 is set to “1”, the Link State-Change Interrupt is enabled.

25.12 – Reserved

25.11 – Auto-Negotiation Error Interrupt Mask

When bit 25.11 is set to “1”, the Auto-Negotiation Error Interrupt is enabled.

25.10 – Auto-Negotiation-Done / Interlock Done Interrupt Mask

When bit 25.10 is set to “1”, the Auto-Negotiation-Done / Interlock Done Interrupt is enabled.

25.9 – Inline Powered Device Detected Interrupt Mask

When bit 25.9 is set to “1”, the Inline Powered Device Detected Interrupt is enabled.

25.8 – Symbol Error Interrupt Mask

When bit 25.8 is set to “1”, the Symbol Error Interrupt is enabled.

25.7 – Descrambler Lock-Lost Interrupt Mask

When bit 25.7 is set to “1”, the Descrambler Lock-Lost Interrupt is enabled.

25.6 – TX FIFO Interrupt Mask

When bit 25.6 is set to “1”, the TX FIFO Interrupt is enabled.

25.5 – RX FIFO Interrupt Mask

When bit 25.5 is set to “1”, the RX FIFO Interrupt is enabled.

25.4 – AMS Media Change Interrupt Mask

When bit 25.4 is set to “1”, the AMS Media Change Interrupt is enabled.

25.3 – False Carrier Interrupt Mask

When bit 25.3 is set to “1”, the False Carrier Interrupt is enabled.

25.2 – Cable Impairment Detect Interrupt Mask[1]

When bit 25.2 is set to “1”, the Cable Impairment Detect Interrupt is enabled.

25.1 – MASTER/SLAVE Resolution Error Interrupt Mask

When bit 25.1 is set to “1”, the MASTER/SLAVE Resolution Error Interrupt is enabled.

25.0 – RXER Interrupt

When bit 25.0 is set to “1”, the RXER Interrupt is enabled.

[1]This interrupt is valid only when the 10/100 speeds are advertised.

25.3.27 Register 26 (1Ah) – Interrupt Status Register

Register 26 (1Ah) – Interrupt Status Register					
Bit	**Name**	**Access**	**States**	**Reset Value**	**Sticky**
15	Interrupt Status	RO SC	1 = Interrupt pending 0 = No interrupt pending	0	
14	Reserved	RO		0	
13	Link State-Change Interrupt Status	RO SC	1 = Link State-Change interrupt pending	0	
12	Reserved	RO		0	
11	Auto-Negotiation Error Interrupt Status	RO SC	1 = Auto-Negotiation Error interrupt pending	0	
10	Auto-Negotiation-Done / Interlock Done Interrupt Status	RO SC	1 = Auto-Negotiation-Done / Interlock Done interrupt pending	0	
9	Inline Powered Device Interrupt Status	RO SC	1 = Inline Powered Device interrupt pending	0	
8	Symbol Error Interrupt Status	RO SC	1 = Symbol Error interrupt pending	0	
7	Descrambler Lock-Lost Interrupt Status	RO SC	1 = Lock-Lost interrupt pending	0	
6	TX FIFO Interrupt Status	RO SC	1 = TX FIFO interrupt pending	0	
5	RX FIFO Interrupt Status	RO SC	1 = RX FIFO interrupt pending	0	
4	AMS Media Change Interrupt Status	RO SC	1 = AMS Media Change interrupt pending	0	
3	False Carrier Detect Interrupt Status	RO SC	1 = False Carrier interrupt pending	0	
2	Cable Impairment Detect Interrupt Status	RO SC	1 = Cable Impairment Detect interrupt pending	0	
1	MASTER/SLAVE Resolution Interrupt Status	RO SC	1 = MASTER/SLAVE Error interrupt pending	0	
0	RXER Interrupt Status	RO	1 = RX_ER interrupt pending 0 = No RX_ER interrupt pending	0	

26.15 – Interrupt Status

When bit 26.15 is set to “1”, an unacknowledged interrupt is pending. The cause of the interrupt can be determined by reading the interrupt status bits in this register. This bit is automatically cleared when read.

26.14 – Reserved

26.13 – Link State-Change Interrupt Status

When the link status of the PHY changes, bit 26.13 is set to “1” if bit 25.13 is also set to “1”. This bit is automatically cleared when read.

26.12 – Reserved

26.11 – Auto-Negotiation Error Interrupt Status

When an error is detected by the Auto-Negotiation state machine, bit 26.11 is set to “1” if bit 25.11 is also set to “1”. This bit is automatically cleared when read.

26.10 – Auto-Negotiation-Done / Interlock Done Interrupt Status

When the Auto-Negotiation state machine finishes a negotiation process, bit 26.10 is set to “1” if bit 25.10 is also set to “1”. This bit is automatically cleared when read.

26.9 – Inline Powered Device Interrupt Status

When a device requiring inline power over CAT-5 is detected, bit 26.9 is set to “1” if bit 25.9 is also set to “1”. This bit is automatically cleared when read.

26.8 – Symbol Error Interrupt Status

When a symbol error is detected by the descrambler, bit 26.8 is set to “1” if bit 25.8 is also set to “1”. This bit is automatically cleared when read.

26.7 – Descrambler Lock-Lost Interrupt Status

When the descrambler loses lock, bit 26.7 is set to “1” if bit 25.7 is also set to “1”. This bit is automatically cleared when read.

26.6 – TX FIFO Interrupt Status

When the TX FIFO enters an underflow or overflow condition, bit 26.6 is set to “1” if bit 25.6 is also set to “1”. This bit is automatically cleared when read.

26.5 – RX FIFO Interrupt Status

When the RX FIFO enters an underflow or overflow condition, bit 26.5 is set to “1” if bit 25.5 is also set to “1”. This bit is automatically cleared when read.

26.4 – AMS Media Change Interrupt Status

When the media type has changed as a result of AMS, bit 26.4 is set to “1” if bit 25.4 is also set to “1”. This bit is automatically cleared when read.

26.3 – False Carrier Detect Interrupt Status

When the PHY has detected a false carrier, bit 26.3 is set to “1” if bit 25.3 is also set to “1”. This bit is automatically cleared when read.

26.2 – Cable Impairment Detect Interrupt Status

When the PHY has detected an impairment on the CAT-5 media, bit 26.3 is set to “1” if bit 25.3 is also set to “1”. This bit is automatically cleared when read.

26.1 – MASTER/SLAVE Resolution Error Interrupt Status

When a MASTER/SLAVE resolution error is detected, bit 26.1 is set to “1” if bit 25.1 is also set to “1”. This bit is automatically cleared when read.

26.0 – RXER Interrupt Status

When an RXER condition occurs, bit 26.0 is set to “1” if bit 25.0 is also set to “1”. This bit is automatically cleared when read.

25.3.28 Register 27 (1Bh) – LED Control Register

Register 27 (1Bh) – LED Control Register

Bit	Name	Access	States	Reset Value	Sticky
15:14	LED Pin 4 Configuration	R/W	00 = Duplex/Collision 01[1] = Activity 10 = Link Fault 11[2]= Tx	CMODE	S
13:12	LED Pin 3 Configuration	R/W	00 = Link/Activity 01[1] = Collision 10 = Fiber Media Selected 11[2] = Rx	CMODE	S
11:10	LED Pin 2 Configuration	R/W	00 = Link10/Activity 01[1] = Duplex/Collision 10 = Link/Activity 11[2] = Tx	CMODE	S
9:8	LED Pin 1 Configuration	R/W	00 = Link100/Activity 01[1] = Link10/100/Activity 10 = Link/Activity 11[2] = Link100/1000/Activity	CMODE	S
7:6	LED Pin 0 Configuration	R/W	00 = Link1000/Activity 01[1] = Link/Activity w/ Serial output on LED pins 1 and 2 10 = Fault 11[2] = Rx	CMODE	S
5	LED Pulse-stretch Rate/ Blink Rate	R/W	0 = 5Hz blink rate/ 200ms pulse-stretch 1 = 10Hz blink rate/ 100ms pulse-stretch	0	S
4	LED Pulsing Enable	R/W	1 = Enable 5kHz, 20% duty cycle LED pulsing for power savings 0 = LED pulsing disabled	CMODE	S
3	LED Pulse-Stretch / Blink Select	R/W	1 = Collision, Activity, Rx and Tx functions will flash at a rate selected by Blink/Pulse-Stretch Rate bits 0 = Collision, Activity, Rx and Tx functions will blink at a rate selected by Blink/Pulse-Stretch Rate bits	0	S
2	Link/Activity Behaviour	R/W	1 = Link function indicates link status only 0 = Link/Activity function will blink or flash when activity is present. Blink/flash behavior is selected by Pulse-Stretch Enable and Blink/Pulse-Stretch Rate bits.	0	S
1	LED Linkxxxx/Activity[3] Behavior	R/W	1 = Link function indicates link status only 0 = All link functions will blink or flash when activity is present. Blink/flash behavior is selected by Pulse-Stretch Enable and Blink/Pulse-Stretch Rate bits.	CMODE	S
0	LED Duplex/Collision Behavior	R/W	1 = Duplex function indicates duplex status only 0 = Duplex function will blink or flash when collision is present	0	S

[1] This setting is 'Force off' when Extended MII Register 20E.13 is set.
[2] This setting is 'Force on' when Extended MII Register 20E.13 is set.
[3] Linkxxxx/Activity stands for Link10/Activity,Link100/Activity,Link1000/Activity,Link10/100/Activity and Link100/1000/Activity. Its definition does not include the Link/Activity function.

27.15:6 – LED Pin Configuration[1]

Each of the five LED pins on each port of the VSC8211 can be configured for one of four functions. These functions are different for each LED pin. Bits 27.15:6 are used to select the function for each LED pin. The reset value of these bits is set by the LED configuration bits in the CMODE hardware configuration. If Extended MII Register 20E.13 is set the LED setting '01' becomes 'Force off' and the LED setting '11' becomes 'Force on'.

27.5 – LED Pulse-Stretch/Blink Rate

The Collision, Activity, Tx and Rx LED functions can be set to either blink at a constant rate or visibly flash through the use of pulse-stretching. The blink rate and pulse-stretch length are set with this bit.

27.4 – LED Pulsing Enable

When bit 27.4 is set to "1", all LED outputs are pulsed at a 5kHz rate with 20% duty cycle in order to save power.

27.3 – LED Pulse-Stretch / Blink Select

When bit 27.3 is set to "1", Collision, Activity, Tx and Rx LED functions will be pulse-stretched. When bit 27.3 is cleared, these LED functions will blink at a constant rate. Bit 27.5 are used to select the pulse-stretch / blink rate.

27.2 – LED Link/Activity Behavior

When bit 27.2 is set to "0", the link status LED function will blink or flash when activity is present. Blink / flash behavior is selected by bits 27.3 and 27.5.

27.1 – LED Linkxxxx/Activity Behavior

When bit 27.1 is set to "0", all linkxxxx status LED functions (Link10, Link100, Link1000, Link10/100, Link100/1000) will blink or flash when activity is present. Blink / flash behavior is selected by bits 27.3 and 27.5.

27.0 – LED Duplex/Collision Behavior

When bit 27.0 is set to "1", the Duplex LED function indicates duplex status only. When bit 27.0 is cleared, the Duplex function will blink or flash when collision is present. Blink / flash behavior is selected by bits 27.3 and 27.5.

[1]Note that if bits 27.7:6 are set to "01", LED pins 1 and 2 are used as serial output pins and the values of bits 27.11:8 are ignored . In 'RTBI/TBI to Fiber Media' Categories of PHY operating modes, MII Register 0.12 must be set for the LEDs to behave according to the settings in MII Register 27.

25.3.29 Register 28 (1Ch) – Auxiliary Control & Status Register

Register 28 (1Ch) – Auxiliary Control & Status Register					
Bit	**Name**	**Access**	**States**	**Reset Value**	**Sticky**
15:7	Reserved	RO		000000000	
6	Enhanced ActiPHY Mode Enable	R/W	1 = Enable enhanced ActiPHY power management 0 = Disable enhanced ActiPHY power management	CMODE	S
5	FDX Status	RO	1 = Full Duplex 0 = Half Duplex	0	
4:3	Speed Status	RO	00 = Speed is 10BASE-T 01 = Speed is 100BASE-TX or 100BASE-FX 10 = Speed is 1000BASE-T 11 = Reserved	00	
2	Reserved[1]	RO		1	
1:0	Enhanced ActiPHY™ Sleep Timer	R/W	00 = 1 second 01 = 2 seconds 10 = 3 seconds 11 = 4 seconds	01	

[1] This bit must always be set to '1'.

28.15:7 – Reserved

28.6 - Enable Enhanced ActiPHY Mode

When bit 28.6 is set to a "1", the Enhanced ActiPHY power management mode is set in the VSC8211. The reset value for this bit is determined by the Enhanced ActiPHY bit in the CMODE hardware configuration.

28.5 – FDX Status

Bit 28.5 indicates the actual FDX/HDX operating mode of the PHY.

28.4:3 – Speed Status

Bits 27.4:3 indicate the actual operating speed of the PHY.

28.2 – Reserved

This bit must always be set to "1".

28.1:0 - Enhanced ActiPHY™ Sleep Timer

This sets the time period the PHY stays in 'Low Power' State when Enhanced ActiPHY™ mode is enabled, before entering the 'LP Wake-up State'. Refer to section 16, "Enhanced ActiPHY Power Management," page 60 for details.

25.3.30 Register 29 (1Dh) – Reserved

Register 29 (1Dh) – Reserved					
Bit	**Name**	**Access**	**States**	**Reset Value**	**Sticky**
15:0	Reserved	RO		00000000 00000000	

29.15:0 - Reserved

25.3.31 Register 30 (1Eh) - MAC Interface Clause 37 Autonegotiation Control & Status

Register 30 (1Eh) – MAC Interface Clause 37 Autonegotiation Control & Status					
Bit	**Name**	**Access**	**States**	**Reset Value**	**Sticky**
15	Reserved	RO		0	
14	Clause 37 Autonegotiation Disable	R/W	1 = Disable clause 37 autonegotiation 0 = Enable clause 37 autonegotiation	0	S
13:12	MAC Remote Fault	RO	Correspond to remote fault bits sent by MAC during clause 37 autonegotiation	00	
11	MAC Asymmetric Pause	RO	Corresponds to Asymmetric Pause bit sent by MAC during clause 37 autonegotiation	0	
10	MAC Symmetric Pause	RO	Corresponds to Symmetric Pause bit sent by MAC during clause 37 autonegotiation	0	
9	Clause 37 Restart Autonegotiaton	R/W SC	1 = Initiate restart of clause 37 autonegotiation 0 = Normal operation	0	
8	MAC Full Duplex	RO	Corresponds to Full Duplex Ability bit sent by MAC during clause 37 autonegotiation	0	
7	MAC Half Duplex	RO	Corresponds to Half Duplex Ability bit sent by MAC during clause 37 autonegotiation	0	
6	Reserved	RO		0	
5	Clause 37 Autonegotiation Complete	RO	1 = Clause 37 autonegotiation has completed successfully 0 = Clause 37 autonegotiation has not completed	0	
4	Reserved	RO		0	
3	Link Interlock Fail	RO	1 = Clause 37/28 autonegotiation interlock could not complete	0	
2	Link Interlock Complete	RO	1 = Clause 37/28 autonegotiation interlock completed	0	
1:0	RXLOS Pulse Delay	R/W	00 = 0ms 01 = 20ms 10 = 200ms 11 = 500ms	01	

30.15 – Reserved

30.14 - Clause 37 Autonegotiation Disable

When bit 30.14 is set to a “1”, the clause 37 auto-negotiation state machine is disabled in the VSC8211. Bit 30.14 is cleared by default.

30.13:12 - MAC Remote Fault

Bits 30.13:12 correspond to the Remote Fault bits sent to the VSC8211 by the MAC during the clause 37 auto-negotiation process.

30.11 - MAC Asymmetric Pause

Bit 30.11 corresponds to the Asymmetric Pause bit sent to the VSC8211 by the MAC during the clause 37 auto-negotiation process.

30.10 - MAC Symmetric Pause

Bit 30.10 corresponds to the Symmetric Pause bit sent to the VSC8211 by the MAC during the clause 37 auto-negotiation process.

30.9 - Clause 37 Restart Autonegotiation

When bit 30.9 is set to a “1”, the clause 37 auto-negotiation process is restarted. This bit is self-clearing and always reads back as “0”.

30.8 - MAC Full Duplex

Bit 30.8 corresponds to the Full Duplex Ability bit sent to the VSC8211 by the MAC during the clause 37 auto-negotiation process.

30.7 - MAC Half Duplex

Bit 30.7 corresponds to the Half Duplex Ability bit sent to the VSC8211 by the MAC during the clause 37 auto-negotiation process.

30.6 - Reserved

30.5 - Clause 37 Autonegotiation Complete

When bit 30.5 is set to a “1”, the clause 37 auto-negotiation has completed successfully.

30.4 - Reserved

30.3 - Link Interlock Fail

Bit 30.3 is set to indicate a failure to complete interlock between Clause-37 auto-negotiation and Clause-28 auto-negotiation. This bit is valid only in SerDes to CAT5 PHY operating modes.

30.2 - Link Interlock Complete

Bit 30.2 is set to indicate a complete interlock between Clause-37 auto-negotiation and Clause-28 auto-negotiation. This bit is valid only in SerDes to CAT5 PHY operating modes.

30.1:0 - RXLOS Pulse Delay

Bits 30.1:0 specify the RXLOS Pulse Delay. It sets the time the RXLOS/SIGDET signal pin is asserted when the CAT5 Media Link is dropped. This bit is only valid when the ‘SFP Mode’ bit Extended MII Register 21E.15 = “1”.

25.3.32 Register 31 (1Fh) – Extended Page Access[1]

Register 31 (1Fh) – Extended Page Access					
Bit	**Name**	**Access**	**States**	**Reset Value**	**Sticky**
15:1	Reserved	RO		000000000000000	
0	Extended Page Access	R/W	1 = MII registers 16:30 will access extended register set 0 = MII registers 16:30 will access standard register set	0	

31.15:0 – Reserved

31.0 - Extended Page Access

In order to provide additional functionality beyond the IEEE802.3 specified 32 MII registers, the VSC8211 contains an extended register set which supports an additional 15 registers. When bit 31.0 is set to a “1”, MII registers 16:30 will access the extended set of registers. The state of bit 31.0 has no effect on MII registers 0:15.

[1]This Register will always read zero.

25.4 Extended MII Registers

25.4.1 Register 16E (10h) - Fiber Media Clause 37 Autonegotiation Control & Status

Register 16E (10h) – Fiber Media Clause 37 Autonegotiation Control & Status

Bit	Name	Access	States	Reset Value	Sticky
15:14	Reserved	RO		00	
13:12	Fiber Remote Fault	RO	Correspond to remote fault bits sent by fiber link partner during clause 37 autonegotiation	00	
11	Fiber Asymmetric Pause	RO	Corresponds to Asymmetric Pause bit sent by fiber link partner during clause 37 autonegotiation	0	
10	Fiber Symmetric Pause	RO	Corresponds to Symmetric Pause bit sent by fiber link partner during clause 37 autonegotiation	0	
9	Clause 37 Restart Autonegotiaton	R/W SC	1 = Initiate restart of clause 37 autonegotiation on fiber media 0 = Normal operation	0	
8	Fiber Full Duplex	RO	Corresponds to Full Duplex Ability bit sent by fiber link partner during clause 37 autonegotiation	0	
7	Fiber Half Duplex	RO	Corresponds to Half Duplex Ability bit sent by fiber link partner during clause 37 autonegotiation	0	
6	Reserved	RO		0	
5	Clause 37 Autonegotiation Complete	RO	1 = Clause 37 autonegotiation has completed successfully with fiber link partner 0 = Clause 37 autonegotiation has not completed with fiber link partner	0	
4	Clause 37 Autonegotiation Autosense Disable	R/W	1 = Clause 37 autonegotiation autosense is disabled 0= Clause 37 autonegotiation autosense is enabled	Depends on PHY Operating Mode	S
3	Reserved	RO		0	
2:1	Remote Fault Mapping Mask	R/W	See section 23, “IEEE802.3 Clause 28/37 Remote Fault Indication Support,” page 77.	01	S
0	Remote Fault Mapping OR	R/W	See section 23, “IEEE802.3 Clause 28/37 Remote Fault Indication Support,” page 77.	1	S

16E.15:14 – Reserved

16.13:12 - Fiber Remote Fault

Bits 16E.13:12 correspond to the Remote Fault bits sent to the VSC8211 by the fiber link partner during the clause 37 auto-negotiation process.

16E.11 - Fiber Asymmetric Pause

Bit 16E.11 corresponds to the Asymmetric Pause bit sent to the VSC8211 by the fiber link partner during the clause 37 auto-negotiation process.

16E.10 - Fiber Symmetric Pause

Bit 16E.10 corresponds to the Symmetric Pause bit sent to the VSC8211 by the fiber link partner during the clause 37 auto-negotiation process.

16E.9 - Clause 37 Restart Autonegotiation

When bit 16E.9 is set to a “1”, the clause 37 auto-negotiation process is restarted with the fiber link partner. This bit is self-clearing and always reads back as “0”.

16E.8 - Fiber Full Duplex

Bit 16E.8 corresponds to the Full Duplex Ability bit sent to the VSC8211 by the fiber link partner during the clause 37 auto-negotiation process.

16E.7 - Fiber Half Duplex

Bit 16E.7 corresponds to the Half Duplex Ability bit sent to the VSC8211 by the fiber link partner during the clause 37 auto-negotiation process.

16E.6 - Reserved

16E.5 - Clause 37 Autonegotiation Complete

When bit 16E.5 is set to a “1”, the clause 37 auto-negotiation has completed successfully.

16E.4 - Clause 37 Autonegotiation Autosense Disable

When bit 16E.1 is cleared, the clause 37 auto-negotiation autosensing ability is enabled.

16E.3 - Reserved

16E.2:1 - Remote Fault Mapping Mask

These bits are used to map between Clause-37 remote fault and Clause-28 remote fault bits. For information about bits 16E.2:1, see section 23, “IEEE802.3 Clause 28/37 Remote Fault Indication Support,” page 77 .

16E.0 - Remote Fault Mapping OR

This bit is used to map between Clause-37 remote fault and Clause-28 remote fault bits. For information about bit 16E.0, see section 23, “IEEE802.3 Clause 28/37 Remote Fault Indication Support,” page 77.

25.4.2 Register 17E (11h) - Serdes Control Register

Register 17E (11h) – SerDes Control Register

Bit	Name	Access	States	Reset Value	Sticky
15:5	Reserved	RO		00000000000	
4:2	RDP/RDN, SCLKP/SCLKN Output Swing Control	R/W	000 = 400mV (peak-to-peak) 001 = 600mV (peak-to-peak) 010 = 800mV (peak-to-peak) 011 = 1.0V (peak-to-peak) 100 = 1.2V (peak-to-peak) 101 = 1.4V (peak-to-peak) 110/111 = 1.6V (peak-to-peak)	100	
1	25mv Hysteresis Disable	R/W	1 = Disable 0 = Enable	Depends on PHY operating Mode	
0	CLKOUTMICRO Enable	R/W	1 = Enable 0 = Disable	1	

17E.15:5 - Reserved

17E.4:2 - RDP/RDN, SCLKP/SCLKN Output Swing Control

These bits set the output swing amplitude (peak-to-peak voltage) on the RDP/RDN and SCLKP/SCLKN output pins.

17E.1 - 25mv Hysteresis Disable

When set, this bit disables the 25mv Hysteresis built into the TDP/TDN and SDIP/SDIN high speed differential input pins. This bit is clear by default in parallel MAC to CAT5/AMS category of PHY Operating modes. This bit is set by default in Serial MAC to CAT5 category of PHY operating modes.

17E.0 - CLKOUTMICRO Enable

When set the CLKOUTMICRO clock output is enabled.

25.4.3 Register 18E (12h) - Reserved

Register 18E (12h) – Reserved

Bit	Name	Access	States	Reset Value	Sticky
15:0	Reserved	RO		00000000 00000000	

18E.15:0 - Reserved

25.4.4 Register 19E (13h) - SerDes Control Register # 2

Register 19E (13h) – Reserved

Bit	Name	Access	States	Reset Value	Sticky
15:2	Reserved	RO		00000000 000000	
1	SIGDET Pin Direction	R/W	0 = Input 1 = Output	CMODE	
0	SIGDET Pin Polarity	R/W	0 = Active High 1 = Active Low	CMODE	

19E.15:2 - Reserved

19E.1 - SIGDET Pin Direction

This bit is valid in non-SFP modes i.e. when MII Register 21E.15 is clear. In non-SFP mode, the RXLOS/SIGDET pin behaves like the SIGDET pin. When set as an input, the assertion of the SIGDET pin enables the SerDes block in Serial MAC to CAT5 category of PHY operating modes. It also triggers the transition to Fiber Media in parallel MAC to AMS category of PHY operating modes. When set as an output, it is asserted when data is driven out of the RDP/RDN pins.

19E.1 - SIGDET Pin Polarity

This bits sets the assertion polarity of the SIGDET pins. This bit is valid in both cases i.e when SIGDET is an input or an output.

25.4.5 Register 20E (14h) - Extended PHY Control Register #3

Register 20E (14h) – Extended PHY Control Register #3					
Bit	**Name**	**Access**	**States**	**Reset Value**	**Sticky**
15	Disable Byte Sync	R/W	0 = Enable 1 = Disable	0	
14	Reserved[1]	RO		0	
13	Enable LED force	R/W	1= Enable LED force 0= Disable LED force	0	S
12:10	SDOP/SDON Output swing Control	R/W	000 = 400mV (peak-to-peak) 001 = 600mV (peak-to-peak) 010 = 800mV (peak-to-peak) 011 = 1.0V (peak-to-peak) 100 = 1.2V (peak-to-peak) 101 = 1.4V (peak-to-peak) 110/111 = 1.6V (peak-to-peak)	100	
9	SDOP/SDON and SDIP/SDIN line impedance	R/W	1 = 75Ω impedance 0 = 50Ω impedance	0	
8	CLKOUTMICRO Frequency	R/W	1 = 125MHz clock output on CLKOUTMICRO 0 = 4MHz clock output on CLKOUTMICRO	CMODE	S
7:6	Media Mode Status	RO	00 = No media selected 01 = Copper media selected 10 = Fiber media selected 11 = Reserved	00	
5	Serial MAC Interface Line Imped-ance	R/W	1 = 75Ω impedance 0 = 50Ω impedance	CMODE	S
4	Enable Link Speed Auto-Downshift	R/W	1 = Enable Link Speed Auto-Downshift 0 = Disable Link Speed Auto-Downshift	0	S
3:2	Link Speed Auto-Downshift Control	R/W	00 = Downshift after 2 failed attempts 01 = Downshift after 3 failed attempts 10 = Downshift after 4 failed attempts 11 = Downshift after 5 failed attempts	01	S
1	Link Speed Auto-Downshift Status	RO	0 = No downshift 1 = Downshift is required or has occurred	0	
0	Reserved	RO		0	

[1] These bits must always be set to “0”.

20E.15 Disable Byte Sync

When enabled, the PHY aligns the 10bit data to the boundary of the COMMA character. This bit is valid only in Serial MAC PHY operating modes.

20E.14 - Reserved

These bits must always be set to ‘”0”.

20E.13 - Enable LED force

When this bit is set, the LED configuration setting “01” becomes ‘Force off’ and the LED configuration setting “11” becomes ‘Force on’. Refer Section 25.3.28: "Register 27 (1Bh) – LED Control Register" for details.

20E.12:10 SDOP/SDON Output swing Control

These bits set the output swing amplitude (peak-to-peak voltage) of the SDOP/SDON high speed differential outputs.

20E.9 SDOP/SDON and SDIP/SDIN line impedance

These bits set the line impedance of the SDOP/SDON and SDIP/SDIN pins to 50Ω or 75Ω single ended (100Ω or 150Ω differential).

20E.8 - CLKOUTMICRO Frequency

The frequency of the CLKOUTMICRO pin can be changed by using bit 20E.8.

20E.7:6 - Media Mode Status

Bits 20E.7:6 reflect the currently active media interface. These bits are most useful for determining the interface currently selected by the Auto Media Sense function. If no link has been established, these bits are cleared.

20E.5 - SerDes Line Impedance

The internal termination impedance of the high speed serial interface inside the VSC8211 can be selected using bit 20E.5. This applies to the SerDes/SGMII pins on the device. The reset value of this bit is determined by the SerDes Line Impedance bit in the CMODE hardware configuration.

20E.4 - Enable Link Speed Auto-Downshift

When bit 20E.4 is set to a “1”, the VSC8211 will “downshift” the autonegotiation advertisement to 100BASE-TX after the number of failed 1000BASE-T auto-negotiation attempts specified in bits 20E.3:2. The reset value of this bit is determined by the Link Speed Downshift bit in the CMODE hardware configuration.

20E.3:2 - Link Speed Auto-Downshift Control

Bits 20E.3:2 determine the number of unsuccessful 1000BASE-T autonegotiation attempts that are required before the auto-negotiation advertisement is “downshifted” to 100BASE-TX. These bits are valid only if bit 20E.4 is set.

20E.1 - Link Speed Auto-Downshift Status

When bit 20E.1 is set to a “1” and bit 20E.4 is set to a “1”, the current link speed is the result of a “downshift” to 100BASE-TX. When bit 20E.1 is set to a “1” and bit 20E.4 is cleared, the current link requires a “downshift” in order to be established.

20E.0 - Reserved

25.4.6 Register 21E (15h) - EEPROM Interface Status and Control Register

Register 21E (15h) - EEPROM Interface Status and Control Register					
Bit	**Name**	**Access**	**States**	**Reset Value**	**Sticky**
15	SFP MODE	R/W	1 = SFP MODE 0 = IEEE MODE	CMODE	SS
14	Re-read EEPROM on Software Reset	R/W	1 = Contents of EEPROM should be re-read on software reset 0 = Contents of EEPROM should not be re-read on software reset	0	SS
13	EEPROM Access Enable	R/W SC	1 = Execute read or write to EEPROM	0	
12	EEPROM Read/Write	R/W	1 = Read from EEPROM 0 = Write to EEPROM	1	
11	EEPROM Ready	RO	1 = EEPROM is ready for read/write 0 = EEPROM is busy	1	
10:0	EEPROM Address	R/W	EEPROM address to read/write	000 00000000	

21E.15 - SFP MODE

SFP Mode (bit 15 = “1”) sets the following PHY defaults:

- TXDIS/$\overline{\text{SRESET}}$ is active high, i.e. behaves like TXDIS.
- MODDEF0/CLKOUTMAC pin functions like MODDEF0, i.e this pin is asserted low by the PHY once the EEPROM interface is released for access through the SMI interface.
- RXLOS/SIGDET pins functions like RXLOS.
- The SMI interface is set in MSA mode.

IEEE Mode (bit 15 = “0”) sets the following PHY defaults:

- TXDIS/$\overline{\text{SRESET}}$ is active low, i.e. behaves like $\overline{\text{SRESET}}$.
- MODDEF0/CLKOUTMAC pin functions like CLKOUTMAC, i.e this pin drives out a 125MHz clock.
- RXLOS/SIGDET pin functions like SIGDET.
- The SMI interface is set in IEEE mode.

21E.14 - Re-Read EEPROM on Software Reset

When bit 21E.14 is set to a “1”, the contents of the EEPROM will be re-read and reloaded into the MII registers upon software reset.

21E.13 - EEPROM Access Enable

When bit 21E.13 is set to a “1”, the EEPROM address in bits 21E.10:0 is written to or read from, based on the state of bit 21E.12. The data to read/write resides in register 22E.

21E.12 - EEPROM Read/Write

When bit 21E.12 is set to a “1”, the VSC8211 will read from the EEPROM when bit 21E.13 is set. When bit 21E.12 is cleared, the VSC8211 will write to the EEPROM when bit 21E.13 is set.

21E.11 - EEPROM Ready

When the VSC8211 is busy reading/writing to the EEPROM, bit 21E.11 will be cleared. Bit 21E.13 should not be set while bit 21E.11 is cleared.

21E.10:1 - EEPROM Address

These bits contain the EEPROM address that the VSC8211 will read from or write to when bit 21E.13 is set.

25.4.7 Register 22E (16h) - EEPROM Data Read/Write Register

Register 22E (16h) - EEPROM Data Read/Write Register

Bit	Name	Access	States	Reset Value	Sticky
15:8	EEPROM Read Data	RO	8-bit data read from EEPROM	00000000	
7:0	EEPROM Write Data	R/W	8-bit data to write to EEPROM	00000000	

22E.15:18 - EEPROM Read Data

After an EEPROM read has occurred by setting bits 21E.13 and 21E.12 to a “1”, the data read from the EEPROM is placed in these bits.

22E.7:0 - EEPROM Write Data

When an EEPROM write is initiated by setting bits 21E.13 to a “1” and clearing bit 21E.12, the data from these bits is written to the EEPROM.

25.4.8 Register 23E (17h) - Extended PHY Control Register #4

Register 23E (17h) - Extended PHY Control Register #4

Bit	Name	Access	States	Reset Value	Sticky
15:11	PHY Address	RO	PHY address latched on reset	CMODE	
10	Enable In-line Powered Device Detection	R/W	1 = In-line powered device detection is enabled 0 = In-line powered device detection is disabled	0	S
9:8	In-line Powered Device Detection Status	RO	00 = Searching for devices 01 = Device found which requires in-line power 10 = Device found which does not require in-line power 11 = Reserved	00	
7:0	CRC Counter	RO SC	CRC counter for Ethernet packet generator	00000000	

23E.15:11 - PHY Address

These bits contain the PHY’s address. The reset value of these bits is determined by the PHY Address bits in the CMODE hardware configuration.

23E.10 - Enable In-line Powered Device Detection

When bit 23E.10 is set to a “1”, the VSC8211 will search for devices requiring CAT-5 in-line power as part of the autonegotiation process.

23E.9:8 - In-line Powered Device Detection Status

Bits 23E.9:8 are used by the station manager to determine if a device which requires in-line power is connected to the VSC8211.

23E.7:0 - CRC Counter

When the Ethernet Packet Generator is enabled, these bits count the number of packets received that contain a CRC error. This counter will saturate at 0FFh and is cleared when read.

25.4.9 Register 24E (18h) - Reserved

Register 24E (18h) - Reserved Register

Bit	Name	Access	States	Reset Value	Sticky
15:0	Reserved	RO		00000000 00000000	

24E.15:0 - Reserved

25.4.10 Register 25E (19h) - Reserved

Register 25E (19h) - Reserved Register

Bit	Name	Access	States	Reset Value	Sticky
15:0	Reserved	RO		00000000 00000000	

25E.15:0 - Reserved

25.4.11 Register 26E (1Ah) - Reserved

Register 26E (1Ah) - Reserved Register

Bit	Name	Access	States	Reset Value	Sticky
15:0	Reserved	RO	-	00000000 00000000	

26E.15:0 - Reserved

25.4.12 Register 27E (1Bh) - Reserved

Register 27E (1Bh) - Reserved Register

Bit	Name	Access	States	Reset Value	Sticky
15:0	Reserved	RO		00000000 00000000	

27E.15:0 - Reserved

25.4.13 Register 28E (1Ch) - Reserved

Register 28E (1Ch) - Reserved Register

Bit	Name	Access	States	Reset Value	Sticky
15:0	Reserved	RO		00000000 00000000	

28E.15:0 - Reserved

25.4.14 Register 29E (1Dh) - 1000BASE-T Ethernet Packet Generator (EPG) Register #1[1]

Register 29E (1Dh) - 1000BASE-T Ethernet Packet Generator (EPG) Register #1					
Bit	**Name**	**Access**	**States**	**Reset Value**	**Sticky**
15	EPG Enable	R/W	1 = Enable EPG 0 = Disable EPG	0	
14	EPG Run/Stop	R/W	1 = Run EPG 0 = Stop EPG	0	
13	Transmission Duration	R/W	1 = Continuous 0 = Send 30,000,000 packets and stop	0	
12:11	Packet Length	R/W	00 = 125 bytes 01 = 64 bytes 10 = 1518 bytes 11 = 10,000 bytes (jumbo packet)	00	
10	Inter-packet Gap	R/W	1 = 8,192 ns 0 = 96 ns	0	
9:6	Destination Address	R/W	MSB's lower nibble of the 6-byte destination address	0001	
5:2	Source Address	R/W	MSB's lower nibble of the 6-byte source address	0000	
1	TXER Control	R/W	1 = Assert TXER 0 = Do not assert TXER	0	
0	Bad FCS Generation	R/W	1 = Generate packets with bad FCS 0 = Generate packets with good FCS	0	

29E.15 - EPG Enable

When bit 29E.15 is set to a "1", the EPG is selected as the driving source for the PHY transmit signals, and the MAC transmit pins are disabled. When bit 29E.15 is cleared, the MAC has full control of the PHY transmit signals.

29E.14 - EPG Run/Stop

Bit 29E.14 controls the beginning and end of packet transmission. When this bit is set to a "1", the EPG begins the transmission of packets. When this bit is cleared, the EPG ends the transmission of packets, after the current packet is transmitted. Bit 29E.14 is valid only if bit 29E.15 is set to a "1".

29E.13 - Transmission Duration

When bit 29E.13 is set to a "1", the EPG will continuously transmit packets as long as bit 29E.14 is set to a "1". If bit 29E.13 is cleared, the EPG will begin transmission of 30,000,000 packets when bit 29E.14 is set to a "1", after which time, bit 29E.14 is automatically cleared. If bit 29E.13 changes during packet transmission, the new value will not take effect until the EPG Run/Stop bit (29E.14) has been cleared and set to a "1" again.

29E.12:11 - Packet Length

Bits 29E.12:11 select the length of the packets to be generated by the EPG. Note that when these bits are set to "11", a 10,000-byte "jumbo" packet is sent, which may not be compatible with all Ethernet equipment. If bits 29E.12:11 change during packet transmission, the new values will not take effect until the EPG Run/Stop bit (29E.14) has been cleared and set to a "1" again.

29E.10 - Inter-packet Gap

Bit 29E.10 selects the inter-packet gap for packets generated by the EPG. If bit 29E.10 changes during packet transmission, the new value will not take effect until the EPG Run/Stop bit (29E.14) has been cleared and set to a "1" again.

[1]Refer section 18.1, "1000BASE-T Ethernet Packet Generator (EPG)," page 64 to for more information.

29E.9:6 - Destination Address

The 6-byte destination address for packets generated by the EPG is assigned one of 16 values in the range 0xF0 FF FF FF FF FFh through 0xFF FF FF FF FF FFh. The most significant byte's lower nibble bits of the destination address are selected by bits 29E.9:6. If bits 29E.9:6 change during packet transmission, the new values will not take effect until the EPG Run/Stop bit (29E.14) has been cleared and set to a "1" again.

29E.5:2 - Source Address

The 6-byte source address for packets generated by the EPG is assigned one of 16 values in the range 0xF0 FF FF FF FF FFh through 0xFF FF FF FF FF FFh. The most significant byte's lower nibble bits are selected by bits 29E.5:2. If bits 29E.5:2 change during packet transmission, the new values will not take effect until the EPG Run/Stop bit (29E.14) has been cleared and set to a "1" again.

29E.1 - TXER Control

When bit 29E.1 is set to a "1", all packets generated by the EPG will have the TXER signal asserted. When this bit is cleared, TXER is not asserted. If bit 29E.1 changes during packet transmission, the new value will not take effect until the EPG Run/Stop bit (29E.14) has been cleared and set to a "1" again.

29E.0 - Bad FCS Generation

When bit 29E.0 is set to a "1", the EPG will generate packets containing an invalid Frame Check Sequence (FCS). When this bit is cleared, the all EPG packets will contain a valid Frame Check Sequence. If bit 29E.0 changes during packet transmission, the new value will not take effect until the EPG Run/Stop bit (29E.14) has been cleared and set to a "1" again.

25.4.15 Register 30E (1Eh) - 1000BASE-T Packet Generator Register #2[1]

Register 30E (1Eh) - 1000BASE-T Packet Generator Register #2

Bit	Name	Access	States	Reset Value	Sticky
15:0	EPG Packet Payload	R/W	Data for packets generated by EPG	00000000 00000000	

30E.15:0 - EPG Packet Payload

Each packet generated by the EPG contains a repeating sequence of bits 30E.15:0 as the data payload. If bits 30E.15:0 change during packet transmission, the new values will not take effect until the EPG Run/Stop bit (29E.14) has been cleared and set to a "1" again.

[1]Refer to section 18.1, "1000BASE-T Ethernet Packet Generator (EPG)," page 64 for more information.

26 Electrical Specifications

26.1 Absolute Maximum Ratings

Stresses listed under the Absolute Maximum Ratings may be applied to devices one at a time without causing permanent damage. Functionality at or above the values listed is not implied. Exposure to these values for extended periods may affect device reliability.

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Table 37. Absolute Maximum Ratings

Symbol	Min	Max	Unit	Parameter Description & Conditions
$T_{Storage}$	-65	150	°C	Storage temperature range.
T_J		+125	°C	Absolute maximum junction temperature.
$VDD33A_{(Analog)}$	-0.5	4.0	V	DC voltage on analog I/O supply pin.
VDDIOMAC/ VDDIOMICRO/ VDDIOCTRL	-0.5	4.0	V	DC voltage on any digital I/O supply pin.
$VDD_{(5V)}$	-0.5	5.5	V	DC voltage on any 5V-tolerant digital input pin.
VDD12	-0.5	1.5	V	DC voltage on any digital core supply pin.
VDD12A	-0.5	1.5	V	DC voltage on 1.2v analog supply pin.
$V_{Pin(DC)}$	-0.5	V_{DD} + 0.5	V	DC voltage on any non-supply pin.
$V_{ESD(HBM)}$	2		kV	ESD voltage on any pin, per event, according to the Human Body Model.
CESD	2		kV	Cable-sourced ESD tolerance, per event, at 200 meters.
$I_{LATCHUP}$	-200	+200	mA	T = +85°C, valid for all I/O signal pins.

ELECTROSTATIC DISCHARGE

This device can be damaged by ESD. Vitesse recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures may adversely affect reliability of the device.

26.2 Recommended Operating Conditions

Table 38. Recommended Operating Conditions

Symbol	Min	Typ	Max	Unit	Parameter Description & Conditions
VDD33A	3.0	3.3	3.6	V	DC voltage on VDD33A pins
VDDIOMAC/ VDDIOMICRO/ VDDIOCTRL	3.0 2.25	3.3 2.5	3.6 2.75	V	DC voltage on VDDIO pins[1]
VDD12	1.14	1.2	1.26	V	DC voltage on VDD12 pins
VDD12A	1.14	1.2	1.26	V	DC voltage on VDD12A pins
F_{REFCLK}		25 125		MHz	Local reference clock (REFCLK) nominal frequency. Refer to F_{TOL} for min. and max. values.
$F_{TOL\ (REFCLK)}$	-100		+100	ppm	Reference clock frequency offset tolerance over specified temperature range (25MHz or 125MHz)
$F_{TOL\ (LINK)}$	-1500		+1500	ppm	CAT5 link partner frequency offset tolerance (for any link speed)[2]
R_{EXT}		2.00		kΩ	External reference circuit bias resistor (1% tolerance).
C_{REF_FILT}		0.1		µF	External reference generator filter capacitor (10% tolerance).
T_{OPER}	0		100	°C	Operating temperature. Lower limit of specification is ambient temperature, and upper limit is case temperature.

[1] On-chip I/O calibration only valid within these recommended operating conditions.

[2] For more information about clocking and frequency offset tolerance specifications when jumbo packet support is required, see the application note *Using Jumbo Packets with SimpliPHYs.*

26.3 Thermal Application Data

Table 39. PCB and Environmental Conditions

Printed Circuit Board Conditions (JEDEC JESD51-9)	
PCB Layers	4
PCB Dimensions (mm x mm)	101.6 x114.3
PCB Thickness (mm)	1.6
Environment Conditions	
Maximum operation junction temperature (ºC)	125
Ambient free-air operating temperature (ºC)	70
Worst Case Power Dissipation (W)	1

Table 40. Thermal Resistance Data

Symbol	Min	Typ	Max	Unit	Parameter Description & Conditions
θ_{JA} (0 m/s air-flow)		37.7		°C/W	Junction-to-ambient thermal resistance
θ_{JA} (1 m/s air-flow)		32.5		°C/W	Junction-to-ambient thermal resistance
θ_{JA} (2 m/s air-flow)		31.1		°C/W	Junction-to-ambient thermal resistance

26.4 Package Thermal Specifications - 117 LBGA

Table 41. Thermal Specifications - 117 ball LBGA 10x14mm package

Symbol	Min	Typ	Max	Unit	Parameter Description & Conditions
T_A		70		°C	Ambient free-air operating temperature
T_J		125		°C	Maximum operating junction temperature
θ_{JC}		15.0		°C/W	Junction-to-case thermal resistance
Ψ_{JT}		0.21		°C/W	Junction-to-top center of case thermal resistance
θ_{JB}		23.0		°C/W	Junction-to-board thermal resistance

26.5 Current and Power Consumption

Power supply current and power consumption information is provided below for PCB design targets. A maximum margin of ±20% from typical should be included to account for variation in the specified power supply voltage ranges, as well as for variation due to the normal silicon process spread and termperature conditons.

Table 42. VDDIO @ 3.3V, RGMII-CAT5, 1000BASE-T, FD, 1518 Byte Random data packet, 100% Utilization, SFP Mode off

Symbol	Min	Typ	Max	Unit	Description
I_{VDD33A}	106	108	110	mA	Analog 3.3V power supply current into VDD33A pins
$I_{VDDIOMAC}$	44	48	52	mA	Digital I/O supply current into VDDIO
$I_{VDDIOCTRL}$	0.5	0.5	0.5	mA	Digital I/O supply current into VDDIOCTRL
$I_{VDDIOMICRO}$	0.5	0.5	0.5	mA	Digital I/O supply current into VDDIOMICRO
I_{VDD12}	291	306	324	mA	Digital 1.2V core power supply current into VDD12 pins
I_{VDD12A}	34	36	38	mA	Analog 1.2V power supply current into VDD12A pins
P_D	823.5	928.5	1042.92	mW	Power Dissipation

Table 43. VDDIO @ 3.3V, RGMII-100BASE-FX, FDX, 1518 Byte Random data packet, 100% Utilization, SFP Mode Off

Symbol	Min	Typ	Max	Unit	Description
I_{VDD12} + I_{VDD12A}		145		mA	Power supply current into VDD12 and VDD12A pins
I_{VDD33A}		96		mA	Analog 3.3V power supply current into VDD33A pins
$I_{VDDIOMAC}$ + $I_{VDDIOCTRL}$ + $I_{VDDIOMICRO}$		19		mA	Digital I/O supply current into VDDIOMAC, VDDIOCTRL, and VDDIOMICRO pins
P_D		554		mW	Power Dissipation

Table 44. VDDIO @ 2.5V, RGMII-CAT5, 1000BASE-T, FD, 1518 Byte Random data packet, 100% Utilization, SFP Mode off

Symbol	Min	Typ	Max	Unit	Description
I_{VDD33A}	106	108	110	mA	Analog 3.3V power supply current into VDD33A pins
$I_{VDDIOMAC}$	33	36	40	mA	Digital I/O supply current into VDDIO
$I_{VDDIOCTRL}$	0.5	0.5	0.5	mA	Digital I/O supply current into VDDIOCTRL
$I_{VDDIOMICRO}$	0.5	0.5	0.5	mA	Digital I/O supply current into VDDIOMICRO
I_{VDD12}	291	306	324	mA	Digital 1.2V core power supply current into VDD12 pins
I_{VDD12A}	34	36	38	mA	Analog 1.2V power supply current into VDD12A pins
P_D	765	859.3	964.87	mW	Power Dissipation

Table 45. VDDIO @ 3.3 V, RGMII-CAT5, 100BASE-TX, FD, 1518 Byte Random data packet, 100% Utilization, SFP Mode off

Symbol	Min	Typ	Max	Unit	Description
I_{VDD33A}	86	88	91.5	mA	Analog 3.3V power supply current into VDD33A pins
$I_{VDDIOMAC}$	16	17	18	mA	Digital I/O supply current into VDDIO
$I_{VDDIOCTRL}$	0.5	0.5	0.5	mA	Digital I/O supply current into VDDIOCTRL
$I_{VDDIOMICRO}$	0.5	0.5	0.5	mA	Digital I/O supply current into VDDIOMICRO
I_{VDD12}	92	98	103	mA	Digital 1.2V core power supply current into VDD12 pins
I_{VDD12A}	24	25	26.5	mA	Analog 1.2V power supply current into VDD12A pins
P_D	441.24	497.4	560.97	mW	Power Dissipation

Table 46. VDDIO @ 2.5 V, RGMII-CAT5, 100BASE-TX, FD, 1518 Byte Random data packet, 100% Utilization, SFP Mode off

Symbol	Min	Typ	Max	Unit	Description
I_{VDD33A}	86	88	91.5	mA	Analog 3.3V power supply current into VDD33A pins
$I_{VDDIOMAC}$	12	13	14	mA	Digital I/O supply current into VDDIO
$I_{VDDIOCTRL}$	0.5	0.5	0.5	mA	Digital I/O supply current into VDDIOCTRL
$I_{VDDIOMICRO}$	0.5	0.5	0.5	mA	Digital I/O supply current into VDDIOMICRO
I_{VDD12}	92	98	103	mA	Digital 1.2V core power supply current into VDD12 pins
I_{VDD12A}	24	25	26.5	mA	Analog 1.2V power supply current into VDD12A pins
P_D	419.49	473	533.82	mW	Power Dissipation

Table 47. VDDIO @ 3.3 V, RGMII-CAT5, 10BASE-T, FD, 1518 Byte Random data packet, 100% Utilization, SFP Mode off

Symbol	Min	Typ	Max	Unit	Description
I_{VDD33A}	146	149	152	mA	Analog 3.3V power supply current into VDD33A pins
$I_{VDDIOMAC}$	11	12.5	13	mA	Digital I/O supply current into VDDIO
$I_{VDDIOCTRL}$	0.5	0.5	0.5	mA	Digital I/O supply current into VDDIOCTRL
$I_{VDDIOMICRO}$	0.5	0.5	0.5	mA	Digital I/O supply current into VDDIOMICRO
I_{VDD12}	27.5	29	31	mA	Digital 1.2V core power supply current into VDD12 pins
I_{VDD12A}	24	24.5	27	mA	Analog 1.2V power supply current into VDD12A pins
P_D	532.71	600.45	670.68	mW	Power Dissipation

Table 48. VDDIO @ 2.5 V, RGMII-CAT5, 10BASE-T, FD, 1518 Byte Random data packet, 100% Utilization, SFP Mode off

Symbol	Min	Typ	Max	Unit	Description
I_{VDD33A}	146	149	152	mA	Analog 3.3V power supply current into VDD33A pins
$I_{VDDIOMAC}$	9	9.5	10	mA	Digital I/O supply current into VDDIO
$I_{VDDIOCTRL}$	0.5	0.5	0.5	mA	Digital I/O supply current into VDDIOCTRL
$I_{VDDIOMICRO}$	0.5	0.5	0.5	mA	Digital I/O supply current into VDDIOMICRO
I_{VDD12}	27.5	29	31	mA	Digital 1.2V core power supply current into VDD12 pins
I_{VDD12A}	24	24.5	27	mA	Analog 1.2V power supply current into VDD12A pins
P_D	519.21	582.15	650.53	mW	Power Dissipation

Table 49. VDDIO @ 3.3 V, RGMII-Fiber, 1000BASE-X, FD, 1518 Byte Random data packet, 100% Utilization, SFP Mode off

Symbol	Min	Typ	Max	Unit	Description
I_{VDD33A}	17	19	20	mA	Analog 3.3V power supply current into VDD33A pins
$I_{VDDIOMAC}$	44	48	52	mA	Digital I/O supply current into VDDIO
$I_{VDDIOCTRL}$	0.5	0.5	0.5	mA	Digital I/O supply current into VDDIOCTRL
$I_{VDDIOMICRO}$	0.5	0.5	0.5	mA	Digital I/O supply current into VDDIOMICRO
I_{VDD12}	51.5	53.5	56.5	mA	Digital 1.2V core power supply current into VDD12 pins
I_{VDD12A}	20	21	23	mA	Analog 1.2V power supply current into VDD12A pins
P_D	267.51	313.8	362.97	mW	Power Dissipation

Table 50. VDDIO @ 2.5 V, RGMII-Fiber, 1000BASE-X, FD, 1518 Byte Random data packet, 100% Utilization, SFP Mode off

Symbol	Min	Typ	Max	Unit	Description
I_{VDD33A}	17	19	20	mA	Analog 3.3V power supply current into VDD33A pins
$I_{VDDIOMAC}$	33	36	40	mA	Digital I/O supply current into VDDIO
$I_{VDDIOCTRL}$	0.5	0.5	0.5	mA	Digital I/O supply current into VDDIOCTRL
$I_{VDDIOMICRO}$	0.5	0.5	0.5	mA	Digital I/O supply current into VDDIOMICRO
I_{VDD12}	51.5	53.5	56.5	mA	Digital 1.2V core power supply current into VDD12 pins
I_{VDD12A}	20	21	23	mA	Analog 1.2V power supply current into VDD12A pins
P_D	209.01	244.6	284.92	mW	Power Dissipation

Table 51. VDDIO @ 3.3 V, SerDes-CAT5, 1000BASE-T, FD, 1518 Byte Random data packet, 100% Utilization, SFP Mode off

Symbol	Min	Typ	Max	Unit	Description
I_{VDD33A}	108	111	112	mA	Analog 3.3V power supply current into VDD33A pins
$I_{VDDIOMAC}$	11	12	13	mA	Digital I/O supply current into VDDIO
$I_{VDDIOCTRL}$	0.5	0.5	0.5	mA	Digital I/O supply current into VDDIOCTRL
$I_{VDDIOMICRO}$	0.5	0.5	0.5	mA	Digital I/O supply current into VDDIOMICRO
I_{VDD12}	308	329	343	mA	Digital 1.2V core power supply current into VDD12 pins
I_{VDD12A}	34	36	37	mA	Analog 1.2V power supply current into VDD12A pins
P_D	749.88	847.2	932.4	mW	Power Dissipation

Table 52. VDDIO @ 2.5 V, SerDes-CAT5, 1000BASE-T, FD, 1518 Byte Random data packet, 100% Utilization, SFP Mode off

Symbol	Min	Typ	Max	Unit	Description
I_{VDD33A}	108	111	112	mA	Analog 3.3V power supply current into VDD33A pins
$I_{VDDIOMAC}$	8	9	10	mA	Digital I/O supply current into VDDIO
$I_{VDDIOCTRL}$	0.5	0.5	0.5	mA	Digital I/O supply current into VDDIOCTRL
$I_{VDDIOMICRO}$	0.5	0.5	0.5	mA	Digital I/O supply current into VDDIOMICRO
I_{VDD12}	308	329	343	mA	Digital 1.2V core power supply current into VDD12 pins
I_{VDD12A}	34	36	37	mA	Analog 1.2V power supply current into VDD12A pins
P_D	734.13	829.3	912.25	mW	Power Dissipation

Table 53. VDDIO @ 3.3 V, SerDes-CAT5, 1000BASE-T, FD, 1518 Byte Random data packet, 100% Utilization, SFP Mode on

Symbol	Min	Typ	Max	Unit	Description
I_{VDD33A}	108	111	112	mA	Analog 3.3V power supply current into VDD33A pins
$I_{VDDIOMAC}$	11	12	13	mA	Digital I/O supply current into VDDIO
$I_{VDDIOCTRL}$	0.5	0.5	0.5	mA	Digital I/O supply current into VDDIOCTRL
$I_{VDDIOMICRO}$	0.5	0.5	0.5	mA	Digital I/O supply current into VDDIOMICRO
I_{VDD12}	258	275	283	mA	Digital 1.2V core power supply current into VDD12 pins
I_{VDD12A}	34	36	37	mA	Analog 1.2V power supply current into VDD12A pins
P_D	692.88	782.4	856.8	mW	Power Dissipation

27 DC Specifications

27.1 Digital Pins (VDDIO = 3.3V)

The following specifications are valid only when $T_{Ambient}$ = 25°C, VDDIO = 3.3V, VDD12 = 1.2V, VDD33A = 3.3V, VSS = 0V.

Table 54. Digital Pins Specifications (VDDIO = 3.3 V)

Symbol	Min	Typ	Max	Unit	Parameter Description & Conditions
V_{OH}	2.4		VDDIO	V	Output high voltage. VDDIO = MIN, I_{OH} = -1.5mA
V_{OL}	GND		0.4	V	Output low voltage. VDDIO = MIN, I_{OL} = 1.5mA
V_{IH}	2.0			V	Input high voltage.
V_{IL}			0.8	V	Input low voltage.
I_{ILeak}	-10		10	µA	Input leakage current.
I_{OLeak}	-10		10	µA	Output leakage current.

27.2 Digital Pins (VDDIO = 2.5V)

The following specifications are valid only when $T_{Ambient}$ = 25°C, VDDIO = 2.5V, VDD12 = 1.2V, VDD33A = 3.3V, VSS = 0V.

Table 55. Digital Pins Specifications (VDDIO = 2.5 V)

Symbol	Min	Typ	Max	Unit	Parameter Description & Conditions
V_{OH}	2.0		VDDIO	V	Output high voltage. VDDIO = MIN, I_{OH} = -1.0mA
V_{OL}	GND		0.4	V	Output low voltage. VDDIO = MIN, I_{OL} = 1.0mA
V_{IH}	1.7			V	Input high voltage. VDDIO = MIN
V_{IL}			0.7	V	Input low voltage. VDDIO = MIN
I_{ILeak}	-10		10	µA	Input leakage current.
I_{OLeak}	-10		10	µA	Output leakage current.

27.3 LED Output Pins (LED[4:0])

The following specifications are valid over a voltage range of 2.3v to 1.3v applied to the LED[4:0] pins.[1]

Table 56. Current Sinking Capability of LED Pins

Symbol	Max	Recommended[1]	Unit	Parameter Description
$I_{sinking}$	40	8	mA	Current sinking Capability of the LED drivers

[1] This recommendation is purely from a power savings view point.

28 Clocking Specifications

28.1 Reference Clock Option

The following component specifications should be used to select a clock reference for use with the VSC8211. For more information about clocking and frequency offset tolerance specifications when jumbo packet support is required, see the application note *Using Jumbo Packets with SimpliPHYs*.

Table 57. Reference Clock Option Specifications

Symbol	Min	Typ	Max	Unit	Parameter Description & Conditions
$F_{TOL-25MHZ}$	-100 ppm	25	+100 ppm	MHz	Total frequency offset tolerance (25MHz clock option), including, initial offset, stability over temperature.
T_{R1}, T_{F1}			4	ns	Rise and fall time (20% to 80%), 25MHz clock option.
T_{R2}, T_{F2}			0.8	ns	Rise and fall time (20% to 80%), 125MHz clock option.
DUTY	45		55	%	Duty cycle (25MHz and 125MHz clock options).

[1] It is assumed that a typical LED will have a forward voltage drop between 1v and 2v, thereby asserting a 1.3v (3.3v-2v) to 2.3v (3.3v-1v) signal across the LED.

28.2 Crystal Option

The following component specifications should be used to select a crystal for use with the VSC8211. For more information about clocking and frequency offset tolerance specifications when jumbo packet support is required, see the application note *Using Jumbo Packets with SimpliPHYs.*

Table 58. Crystal Option Specifications

Symbol	Min	Typ	Max	Unit	Parameter Description & Conditions
F_{REF}		25		MHz	Fundamental mode, AT-cut type, parallel resonant crystal reference frequency.
$F_{TOL(TOTAL)}$	-50		+50	ppm	Fundamental mode, AT-cut type, parallel resonant crystal total frequency offset, including, initial offset, stability over temperature, aging and capacitive loading.
C_L	18		20	pF	Crystal parallel load capacitance.
C_{L-EXT}		30		pF	Crystal external load capacitors to GND.[1]
ESR		10	30	Ω	Equivalent Series Resistance of crystal.
P_D			0.5	mW	Crystal oscillator drive level.

[1] These values can depend on board parasitics.

29 SerDes Specifications

The following specifications are valid over the recommended operating conditions listed in Table 38.

Table 59. SerDes Specifications

Symbol	Min	Typ	Max	Unit	Parameter Description & Conditions
T_lock		500		uS	Frequency Lock Time
Vidiff	100		2400	mV	Peak to peak differential voltage (TDP-TDN) terminated with a 100Ω (differential) Load
Vodiff	350	1200	1400	mV	Peak to peak differential voltage (RDP-RDN), 100Ω (differential) termination in the module, recommended voltage range is 500mV-1200mV
Vicm	0.437 x VDD12	.45 x VDD12	0.464 x VDD12	V	Input common mode voltage
Vocm	0.4 x VDD12	.45 x VDD12	0.5 x VDD12	V	Output common mode voltage
Tr_HS / Tf_HS			300	ps	20%-80% Transition time. Trise / Tfall of high speed output driver.
RJ		4		ps RMS	Random Jitter (1 sigma) as per 802.3 Standard. Random Jitter component at RDP, RDN in Parallel MAC to Fiber Media category of PHY operating modes.
DJ		30		ps pk-pk	With a K28.5+/K28.5- Pattern. Deterministic Jitter at RDP, RDN in Parallel MAC to Fiber Media category of PHY operating modes.
RJ		18		ps RMS	Random Jitter (1 sigma) as per 802.3 Standard. Random Jitter component at RDP, RDN in Serial MAC to CAT5 Media category of PHY operating modes.
DJ		38		ps pk-pk	With a K28.5+/K28.5- Pattern. Deterministic Jitter at RDP, RDN in Serial MAC to CAT5 Media category of PHY operating modes.
SerDes Data Rate	1249.375	1250	1250.625	Mbps	SerDes data rate (+/- 500ppm)

30 System Timing Specifications

30.1 GMII Mode Transmit Timing (1000BASE-T)

For GMII mode, the following specifications are valid when the I/O power supply (VDDIOMAC) is 2.5V or 3.3V, ±10%, and the MAC/Media Interface Mode Select bits (see section 25.3.24 “Register 23 (17h) – PHY Control Register #1,” page 108) have been set to GMII mode.

Table 60. GMII Mode Transmit Timing (1000BASE-T) Specifications

Symbol	Min	Typ	Max	Unit	Parameter Description & Conditions
$T_{GTXCLK\text{-}Period}$		8.0		ns	GTXCLK clock period.
$F_{TOL\text{-}GTXCLK}$	-100		+100	ppm	GTXCLK frequency offset tolerance.
$T_{GTXCLK\text{-}High}$	2.5			ns	GTXCLK minimum pulse width high.
$T_{GTXCLK\text{-}Low}$	2.5			ns	GTXCLK minimum pulse width low.
$T_{GTXCLK\text{-}Setup}$	2.0			ns	GMII data TXD[7:0], TXER, TXEN setup time.
$T_{GTXCLK\text{-}Hold}$	0.0			ns	GMII data TXD[7:0], TXER, TXEN hold time.
t_R			1.0	ns	GTXCLK clock rise time, measured from 0.7V to 1.9V.
t_F			1.0	ns	GTXCLK clock fall time, measured from 0.7V to 1.9V.

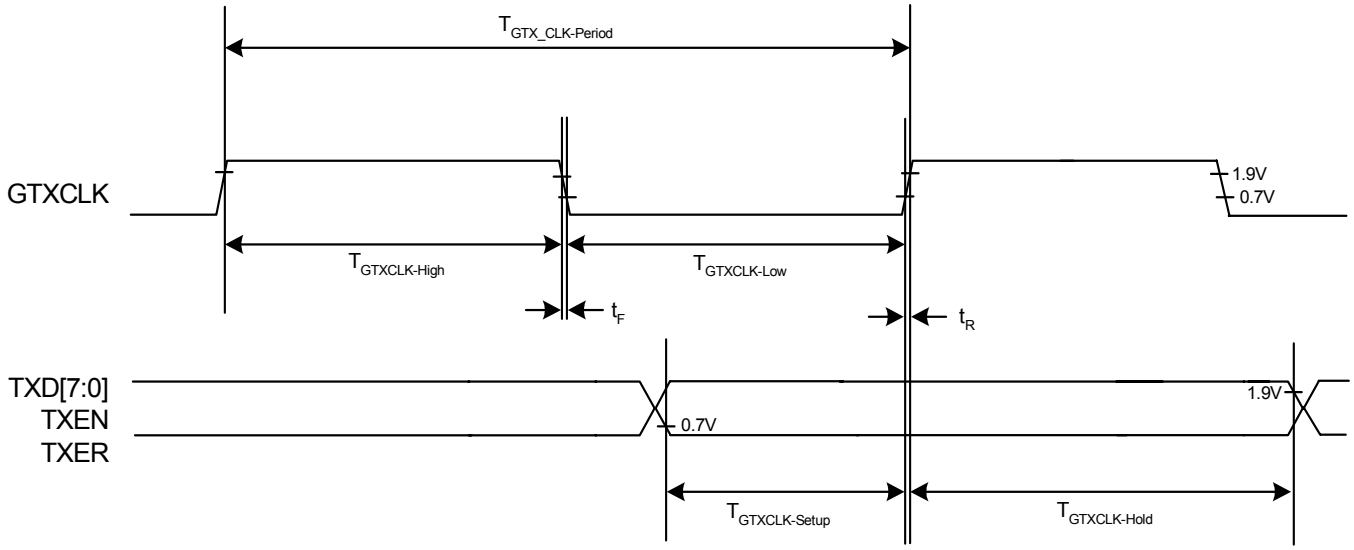

Figure 37. GMII Transmit AC Timing in 1000BASE-T Mode

30.2 GMII Mode Receive Timing (1000BASE-T)

For GMII mode, the following specifications are valid when the I/O power supply (VDDIOMAC) is 2.5V or 3.3V, ±10%, and the MAC/Media Interface Mode Select bits (see section 25.4.8 “Register 23E (17h) - Extended PHY Control Register #4,” page 129) have been set to GMII mode.

Table 61. GMII Mode Receive Timing (1000BASE-T) Specifications

Symbol	Min	Typ	Max	Unit	Parameter Description & Conditions
Symbol	**Min**	**Typ**	**Max**	**Unit**	**Parameter Description & Conditions**
$T_{RXCLK\text{-}Period}$		8.0		ns	RXCLK clock period.
$F_{TOL\text{-}RXCLK}$	-100		+100	ppm	RXCLK frequency offset tolerance.
$T_{RXCLK\text{-}High}$	2.5			ns	RXCLK minimum pulse width high.
$T_{RXCLK\text{-}Low}$	2.5			ns	RXCLK minimum pulse width low.
$T_{RXCLK\text{-}Setup}$	2.5			ns	RXD[7:0], RXDV, RXER setup time to RXCLK
$T_{RXCLK\text{-}Hold}$	0.5			ns	RXD[7:0], RXDV, RXER hold time to RXCLK
t_R			1.0	ns	RXCLK clock rise time, measured from 0.7V to 1.9V.
t_F			1.0	ns	RXCLK clock fall time, measured from 0.7V to 1.9V.

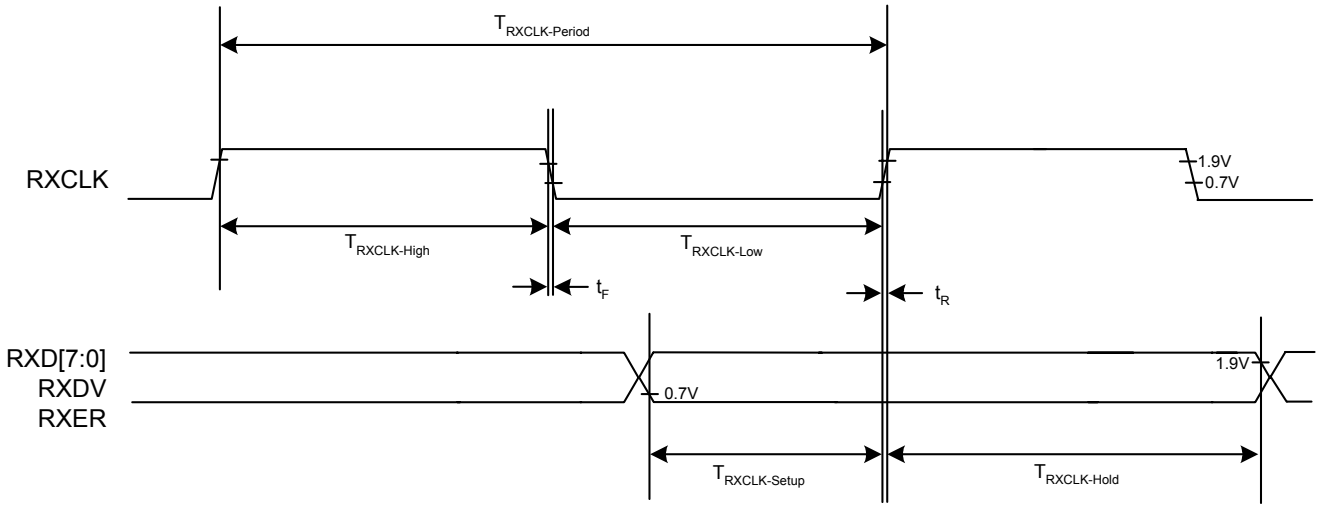

Figure 38. GMII Receive AC Timing in 1000BASE-T Mode

30.3 MII Transmit Timing (100Mbps)

The following specifications are valid when the I/O power supply (VDDIOMAC) is 2.5V or 3.3V, ±10%, the MAC/Media Interface Mode Select bits (see section 25.4.8 “Register 23E (17h) - Extended PHY Control Register #4,” page 129) have been set to GMII/MII mode and the PHY is linked up in 100BASE-T.

Table 62. MII Transmit AC Timing Specifications (100 Mbps)

Symbol	Min	Typ	Max	Unit	Parameter Description & Conditions
$T_{TXCLK\text{-}Delay}$	0		25	ns	Delay from TXCLK to TXD[3:0], TXEN, TXER.
$T_{TXCLK\text{-}Duty}$	35		65	%	TXCLK duty cycle.

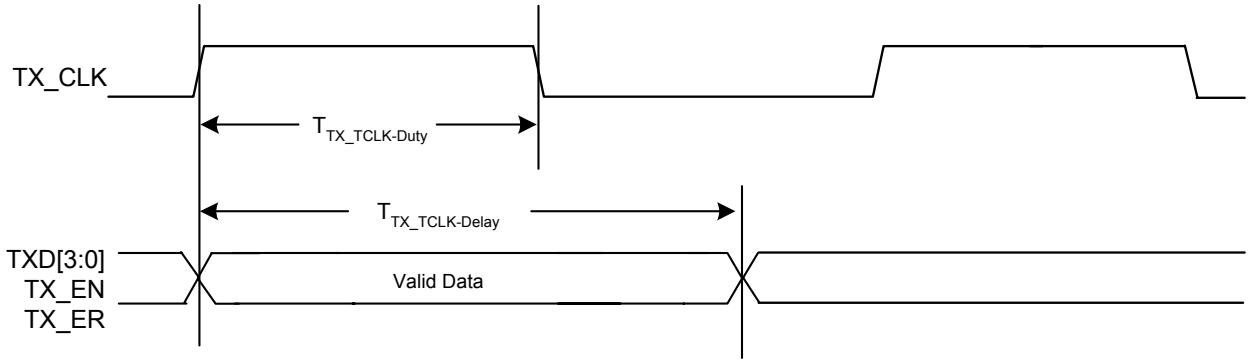

Figure 39. MII Transmit AC Timing (100Mbps)

30.4 MII Receive Timing (100Mbps)

The following specifications are valid when the I/O power supply (VDDIOMAC) is 2.5V or 3.3V, ±10%, the MAC/Media Interface Mode Select bits (see section 25.4.8 “Register 23E (17h) - Extended PHY Control Register #4,” page 129) have been set to GMII/MII mode and the PHY is linked up in 100BASE-T.

Table 63. MII Receive Timing Specifications (100 Mbps)

Symbol	Min	Typ	Max	Unit	Parameter Description & Conditions
$T_{RXCLK\text{-}Setup}$	10			ns	RXD[3:0], RXDV, RXER setup time to RXCLK.
$T_{RXCLK\text{-}Hold}$	10			ns	RXD[3:0], RXDV, RXER hold time to RXCLK.

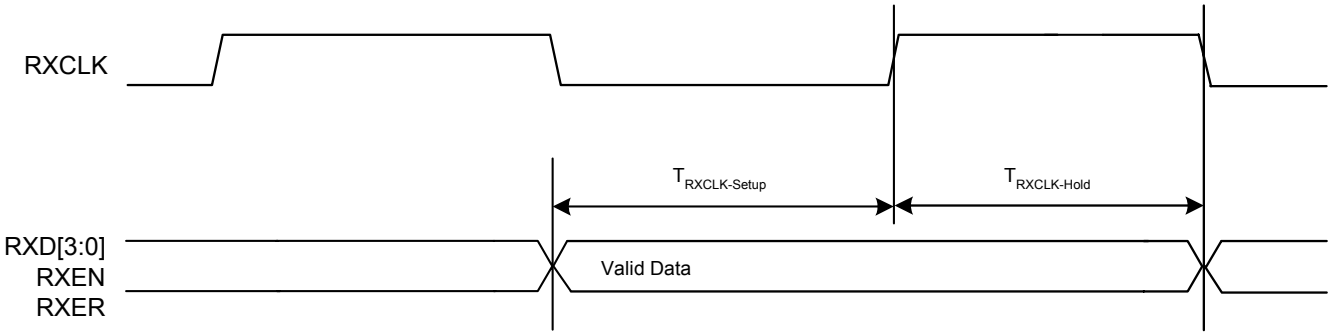

Figure 40. MII Receive AC Timing (100Mbps)

30.5 TBI Mode Transmit Timing

The following specifications are valid when the I/O power supply (VDDIOMAC) is 2.5V or 3.3V, ±5%, per the RGMII v2.0 specification, and the MAC/Media Interface Mode Select bits (see section 25.4.8 “Register 23E (17h) - Extended PHY Control Register #4,” page 129) have been set to TBI mode.

Table 64. TBI Mode Transmit Timing

Symbol	Min	Typ	Max	Unit	Parameter Description & Conditions
$T_{PMA_TX_CLK}$	8.0 - 100ppm	8.0	8.0 + 100ppm	ns	PMA transmit clock period
T_{SETUP}	2			ns	Transmit data setup time to rising edge of PMA_TX_CLK.
T_{HOLD}	1			ns	Transmit data hold time to rising edge of PMA_TX_CLK.
T_{DUTY}	40		60	%	PMA_TX_CLK duty cycle.
t_R	0.7		2.4	ns	Clock rise time (0.8V to 2.0V).
t_F	0.7		2.4	ns	Clock fall time (2.0V to 0.8V).
t_R	0.7			ns	Data rise time (0.8V to 2.0V).
t_F	0.7			ns	Data fall time (2.0V to 0.8V).

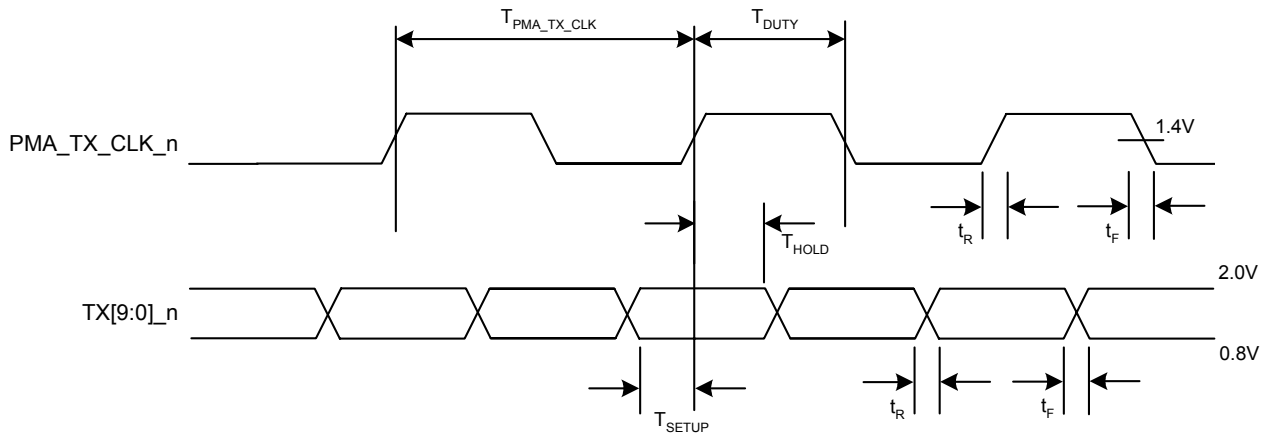

Figure 41. TBI Transmit AC Timing

30.6 TBI Mode Receive Timing

The following specifications are valid when the I/O power supply (VDDIOMAC) is 2.5V or 3.3V, ±5%, per the RGMII v2.0 specification, and the MAC/Media Interface Mode Select bits (see section 25.4.8 “Register 23E (17h) - Extended PHY Control Register #4,” page 129) have been set to TBI mode.

Table 65. TBI Mode Receive Timing

Symbol	Min	Typ	Max	Unit	Parameter Description & Conditions
$T_{PMA_RX_CLK}$		62.5		MHz	PMA receive clock frequency (PMA_RX_CLK1 and PMA_RX_CLK0).
T_{DRIFT}	0.2			µs/MHz	PMA_RX_CLK drift rate.[1]
T_{A-B}	7.5		8.5	ns	PMA_RX_CLK skew.
T_{SETUP}	2.5			ns	Receive data setup time to rising edge of PMA_RX_CLK.
T_{HOLD}	1.5			ns	Receive data hold time to rising edge of PMA_RX_CLK.
T_{DUTY}	40		60	%	PMA_RX_CLK duty cycle.
t_R	0.7		2.4	ns	Clock rise time (0.8V to 2.0V).
t_F	0.7		2.4	ns	Clock fall time (2.0V to 0.8V).
t_R	0.7			ns	Data rise time (0.8V to 2.0V).
t_F	0.7			ns	Data fall time (2.0V to 0.8V).

[1] The drift rate is the (minimum) time for PMA_RX_CLK to drift from 63.5MHz to 64.5MHz or 60MHz to 59MHz from the PMA_RX_CLK lock value. It is applicable under all input signal conditions (except during code-group alignment), provided that the receiver clock recovery unit was previously locked to PMA_TX_CLK or to a valid input signal.

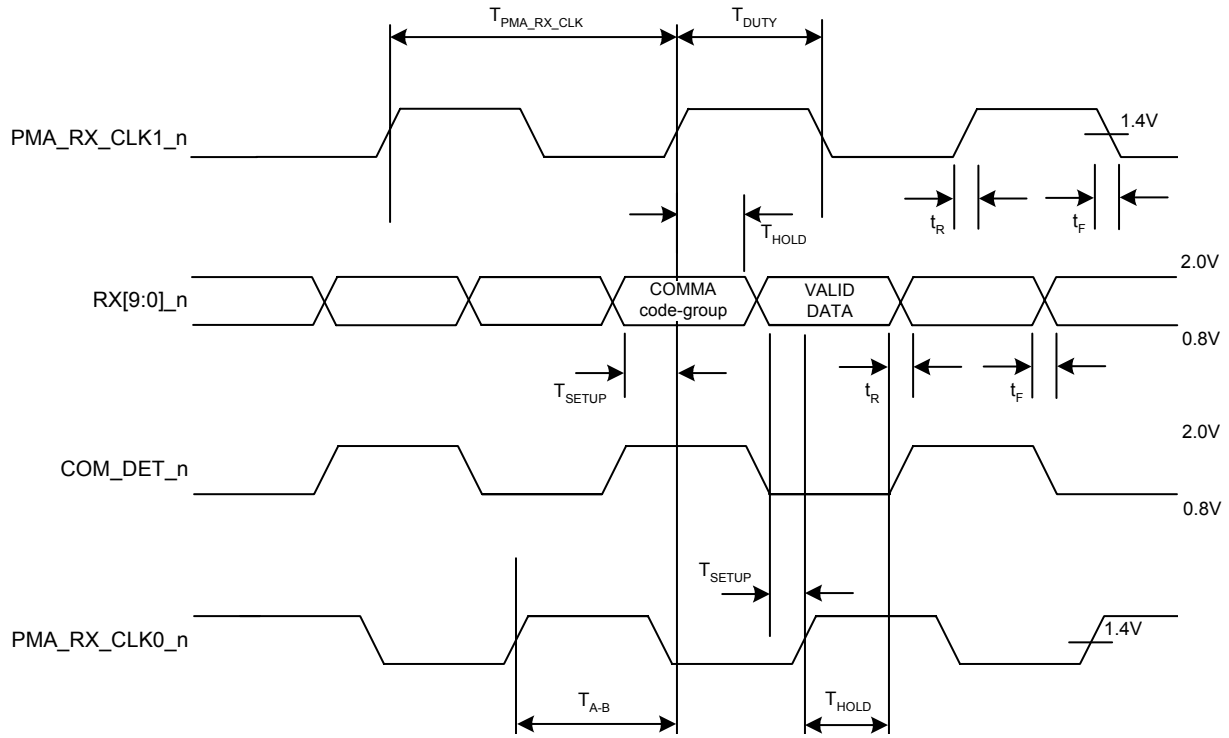

Figure 42. TBI Receive AC Timing

30.7 RGMII/RTBI Mode Timing

For RGMII/RTBI modes, the following specifications are valid when the I/O power supply (VDDIOMAC) is 2.5V or 3.3V, ±5%, per the RGMII v2.0 specification, and the MAC/Media Interface Mode Select bits (see section 25.4.8 “Register 23E (17h) - Extended PHY Control Register #4,” page 129) have been set to RGMII/RTBI mode.

Table 66. RGMII/RTBI Mode Timing

Symbol	Min	Typ	Max	Unit	Parameter Description & Conditions
$T_{skew}T$	-500	0	500	ps	Data to clock output skew (at PHY) – uncompensated mode
$T_{skew}R$	1	1.8	2.6	ns	Data to clock output skew (at receiver) – uncompensated mode[1]
$T_{setup}T$	1.2	2.0	0	ns	Data to clock output Setup (at PHY integrated delay)[2]
$T_{hold}T$	1.2	2.0	0	ns	Data to clock output Setup (at transmitter integrated delay)[2]
$T_{setup}R$	1.0	2.0	0	ns	Data to clock output Setup (at receiver integrated delay)[2]
$T_{hold}R$	1.0	2.0	0	ns	Data to clock output Setup (at PHY integrated delay)[2]
$T_{CYC1000}$ T_{CYC100} T_{CYC10}	7.2 36 360	8 40 400	8.8 44 440	ns	Clock cycle duration
$Duty_{1000}$	45	50	55	%	Duty cycle for 1000BASE-T[3]
$Duty_{10/100}$	40	50	60	%	Duty cycle for 10BASE-T and 100BASE-TX[3]
T_R, T_F			.75	ns	Rise, fall time (20% to 80%)
$V_{thresh1.5}$ $V_{thresh2.5}$ $V_{thresh3.3}$		0.75 1.25 1.65		V V V	TXCLK Switching Threshold based on VDDIOMAC

[1] This implies that PC board design will require clocks to be routed such that an additional trace delay of greater than 1.5ns and less than 2.0ns will be added to the associated clock signal. This is normal operating mode (RGMII timing is not compensated). To enable RGMII timing compensation, see MII Register 23.11:8.

[2] RGMII-ID mode (RGMII with Internal Delay Compensation On) - a programmable delay of 0ns, 1.5ns, 2.0ns, or 2.5ns is added to the TXC and RXC signals inside the PHY. Each of delays is independently programmable using MII register 23.11:8.

[3] Duty cycle may be stretched or shrunk during speed changes or while transitioning to a received packet’s clock domain, as long as the minimum duty cycle is not violated, and stretching occurs for no more than three T_{CYC} of the lowest speed transitioned between.

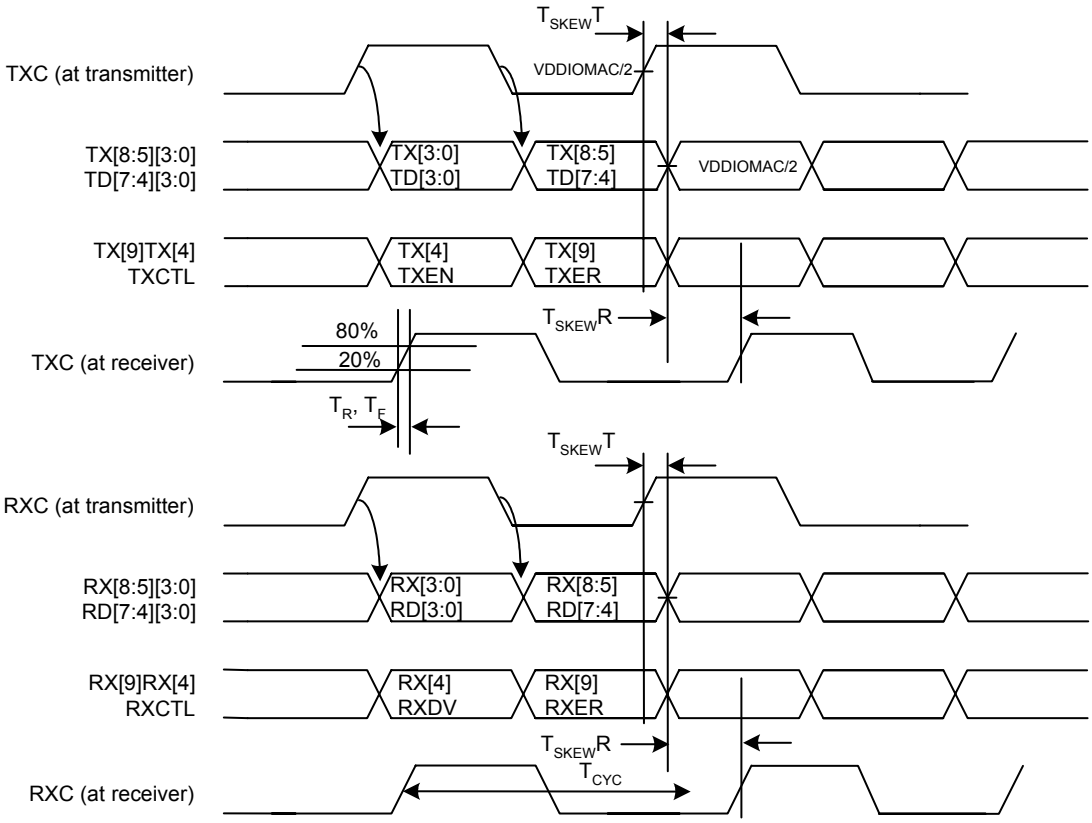

Figure 43. RGMII/RTBI Uncompensated AC Timing and Multiplexing

The RGMII specification (v2.0) defines the relationship shown above between the clock and data signals at the MAC/PHY interface.

To meet this timing specification, a 1.5ns delay to the TXCLK and RXCLK signals is typically added on the PC board using a long “trombone shaped” trace.

The VSC8211 includes an optional mode of operation where this PCB delay is handled internally (on-chip). This operating mode can be enabled by setting MII Register 23.11:8. The internal delay on the TXCLK and RXCLK clocks can be independently controlled to be 0ns, 1.5ns, 2.0ns, or 2.5ns. When the internal delay feature is used, the PHY is said to be in “RGMII Compensated Mode”.

In this operating mode, the VSC8211 expects the following relationship between TXCLK and TD on the transmit side and RXCLK and RD on the receive side (assuming internal delay on the transmit side and receive side internal delay set to 2.0ns):

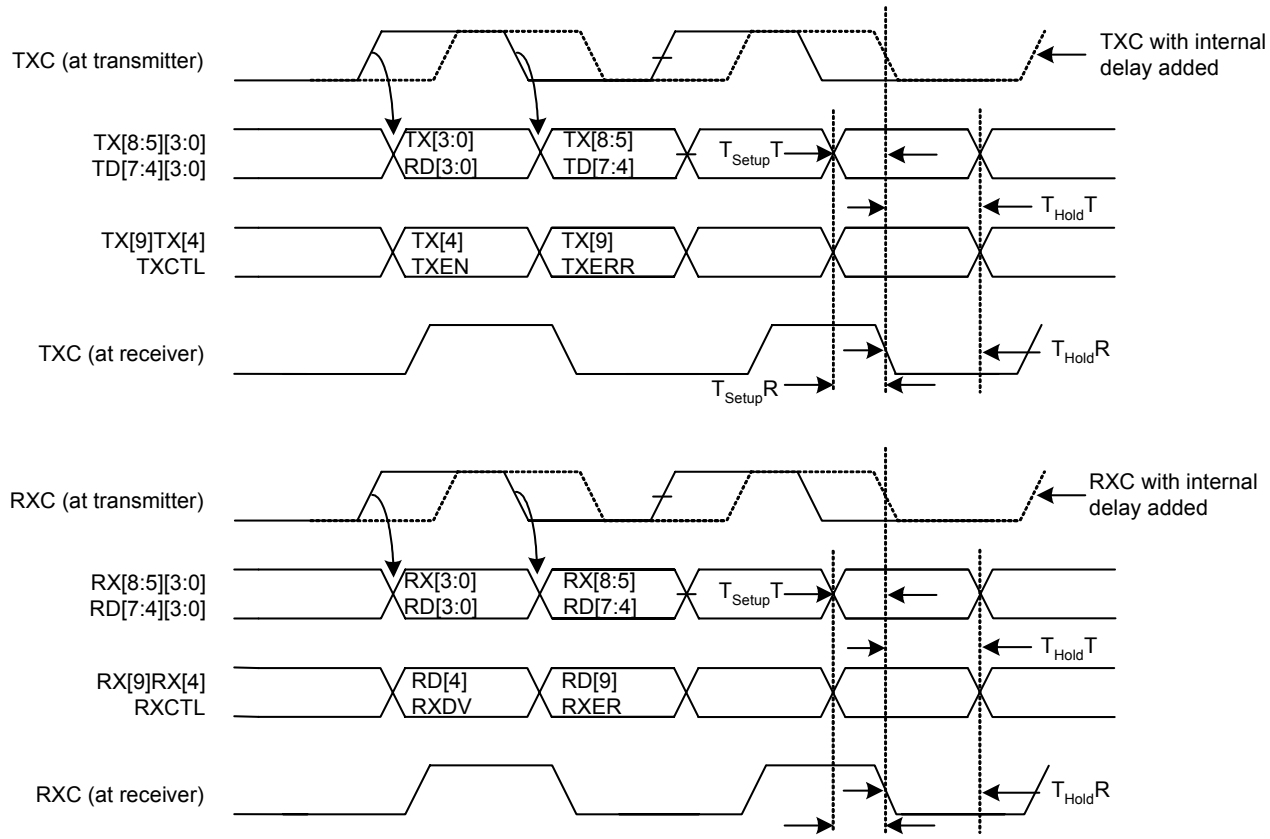

Figure 44. RGMII/RTBI Compensated AC Timing and Multiplexing

No “trombone shaped” traces are required when using this approach. Advantages of this compensated timing over RGMII v2.0:

- Simplified board design
- More compact routes (less board area)
- Lower EMI emissions
- Greater possible distance between MAC and PHY (simplifying design and layout)
- Improved signal integrity at a given distance between the MAC and PHY

30.8 JTAG Timing

The following specifications are valid only when the I/O power supply (VDDIOCTRL) is at either 3.3V, ±5%, or 2.5V, ±5%.

Table 67. JTAG Timing

Symbol	Min	Typ	Max	Unit	Parameter Description & Conditions
$T_{TCK\text{-}Period}$	100			ns	TCK period.
$T_{TCK\text{-}High}$	45			ns	TCK minimum pulse width high.
$T_{TCK\text{-}Low}$	45			ns	TCK minimum pulse width low.
$T_{TDI/TMS\text{-}Setup}$	10			ns	(TMS or TDI) to TCK setup time.
$T_{TDI/TMS\text{-}Hold}$	10			ns	(TMS or TDI) to TCK hold time.
$T_{TDO\text{-}Delay}$			15	ns	TDO delay from TCK.

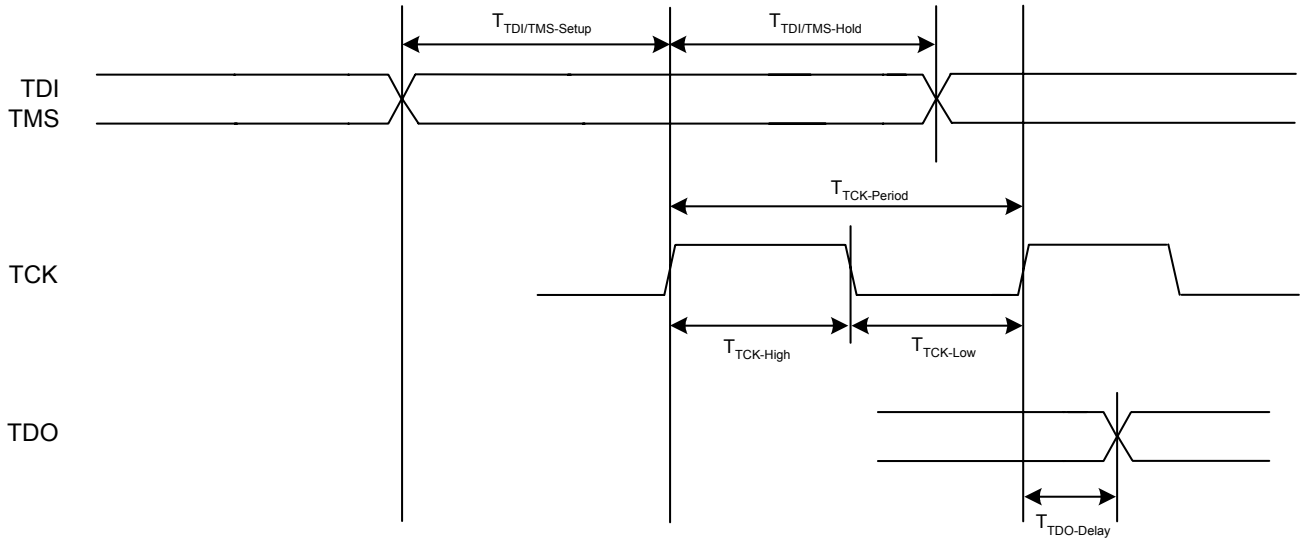

Figure 45. JTAG Interface AC Timing

30.9 SMI Timing

The following specifications are valid only when the I/O power supply (VDDIOMICRO) is at either 3.3V, ±5%, or 2.5V, ±5%.

Table 68. SMI Timing

Symbol	Min	Typ	Max	Unit	Parameter Description & Conditions
F_{MDC}	0	2.5	12.5	MHz	MDC clock frequency.
$T_{MDC\text{-}High}$	20	50		ns	MDC clock pulse width high.
$T_{MDC\text{-}Low}$	20	50		ns	MDC clock pulse width low.
$T_{MDIO\text{-}Setup}$	10			ns	MDIO to MDC setup time when sourced by Station Manager.
$T_{MDIO\text{-}Hold}$	10			ns	MDIO to MDC hold time when sourced by Station Manager.
$T_{MDIO\text{-}Delay}$		10	300	ns	MDC to MDIO delay time from VSC8211. Delay will depend on value of external pull-up resistor on MDIO pin.

Note: A 4.7kΩ to 10kΩ pull-up or pull-down is recommended on the $\overline{\text{MDINT}}$ pin.

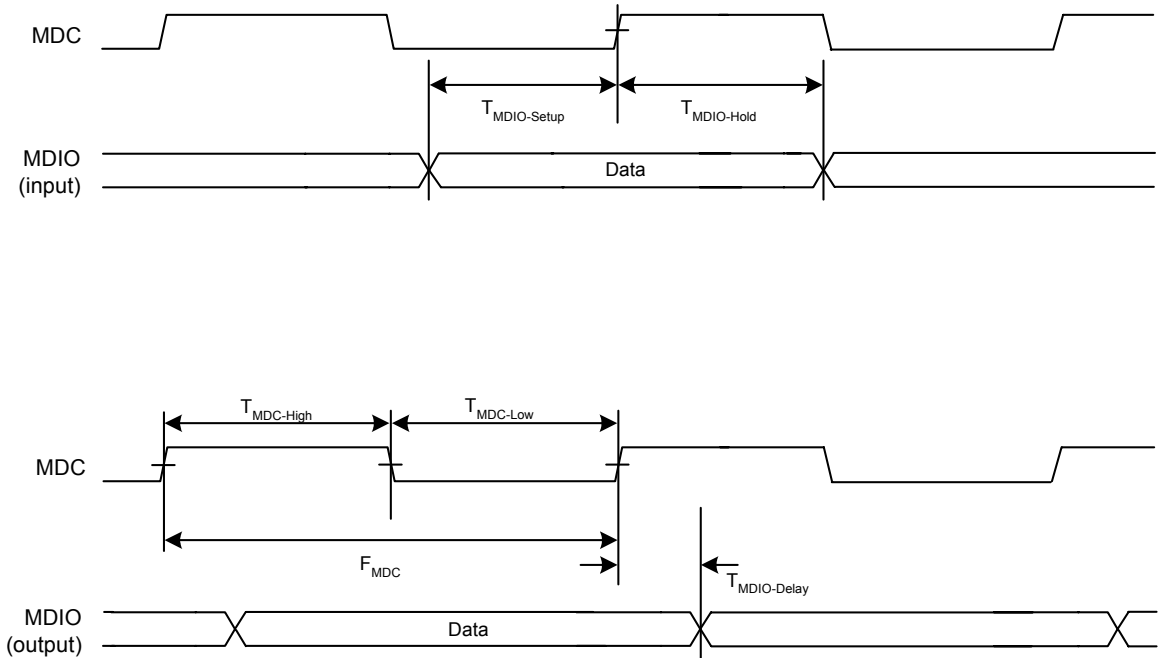

Figure 46. SMI AC Timing

30.10 $\overline{\text{MDINT}}$ Timing

The following specifications are valid only when the I/O power supply (VDDIOMICRO) is at either 3.3V, ±5%, or 2.5V, ±5%.

Table 69. $\overline{\text{MDINT}}$ Timing

Symbol	Min	Typ	Max	Unit	Parameter Description & Conditions
t_F			110	ns	$\overline{\text{MDINT}}$ fall time, assuming a 2.2kΩ external pull-up resistor and a 50pF total capacitive load.

30.11 Serial LED_CLK and LED_DATA Timing

The following specifications are valid only when the I/O power supply (VDD33A) is at 3.3V, ±5%.

Table 70. Serial LED_CLK and LED_DATA Timing

Symbol	Min	Typ	Max	Unit	Parameter Description & Conditions
T_{LED_CLK}		1		µs	LED_CLK output period.
$T_{LED_CLK\text{-}Pause}$		25		ms	LED_CLK pause between LED bit sequence repeat (un-preambled mode).
$T_{LED_DATA\text{-}Delay}$		0.5		µs	LED_DATA propagation delay from rising edge of LED_CLK.

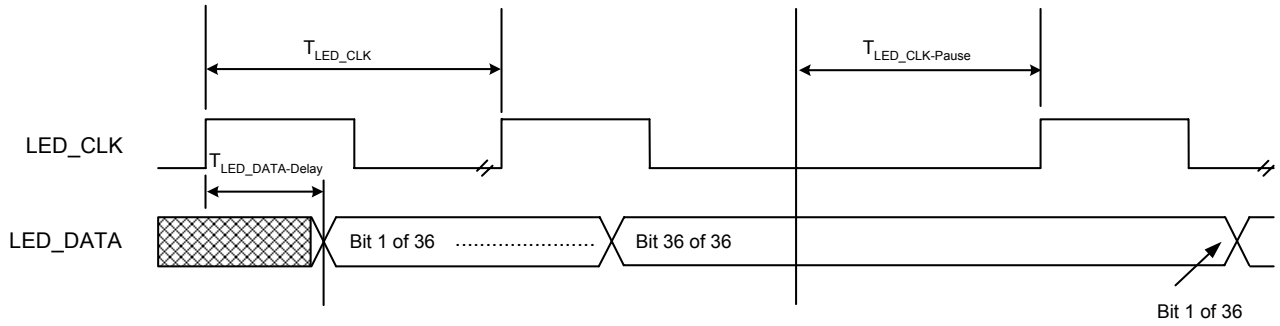

Figure 47. LED_CLK and LED_DATA Output AC Timing

30.12 REFCLK Timing

The following specifications are valid only when the VDD33A is at 3.3V, ±5%. For more information about clocking and frequency offset tolerance specifications when jumbo packet support is required, see the application note *Using Jumbo Packets with SimpliPHYs.*

Table 71. REFCLK Timing

Symbol	Min	Typ	Max	Unit	Parameter Description & Conditions
$T_{REFCLK25}$		40		ns	Reference clock period, PLLMODE = 0 (25MHz reference).
$T_{REFCLK125}$		8		ns	Reference clock period, PLLMODE = 1 (125MHz reference).
$F_{STABILITY}$			50	ppm	Reference clock frequency stability (0°C to 70°C).
T_{DUTY}	40	50	60	%	REFCLK duty cycle in both 25MHz and 125MHz modes.
$J_{REFCLK25}$, $J_{REFCLK125}$			300	ps	Total jitter of 25MHz or 125MHz reference clock (peak-to-peak).
$t_{R/F\ (REFCLK25)}$			4	ns	Reference clock rise time, 25MHz mode (20% to 80%).
$t_{R/F\ (REFCLK125)}$			1	ns	Reference clock rise time, 125MHz mode (20% to 80%).

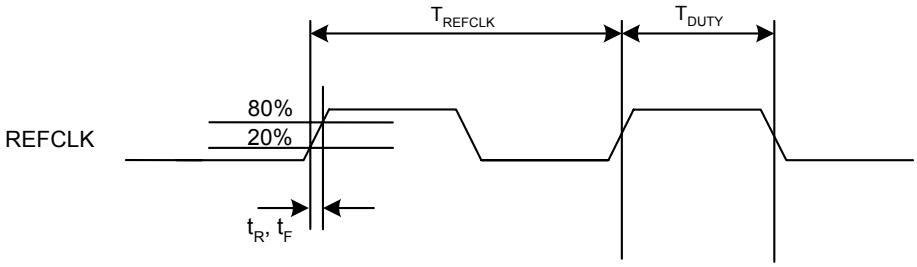

Figure 48. REFCLK AC Timing

30.13 CLKOUTMAC and CLKOUTMICRO Timing

The following specifications are valid only when the I/O power supply (VDDIOMAC for CLKOUTMAC and VDDIOMICRO for CLKOUTMICRO) is at either 3.3V ±5%, or 2.5V ±5%.
.

Table 72. CLKOUTMAC and CLKOUTMICRO Timing

Symbol	Min	Typ	Max	Unit	Parameter Description & Conditions
$T_{CLKOUTMAC}$		8		ns	Clock period.
$T_{CLKOUTMICRO}$		250 8		ns	Clock period. Either 4MHz, or 125MHz
$F_{STABILITY}$			50	ppm	Clock frequency stability (0°C to 70°C).
T_{DUTY}	40	50	60	%	Clock duty cycle.
J_{CLK125}			300	ps	Total jitter of clock (peak-to-peak).
$t_{R/F\ (CLK125)}$			1	ns	Clock rise time (20% to 80%).

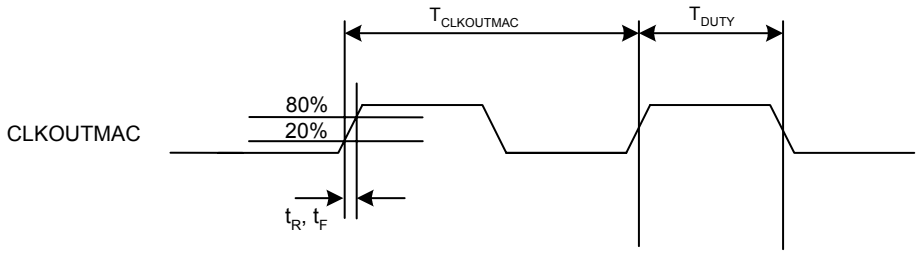

Figure 49. CLKOUTMAC AC Timing

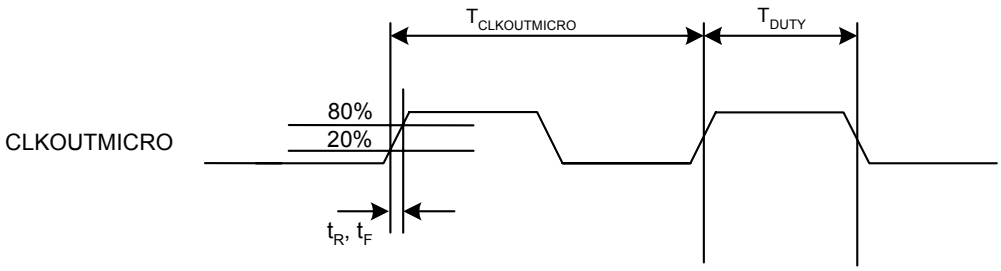

Figure 50. CLKOUTMICRO AC Timing

30.14 Reset Timing

The following specifications are valid only when the I/O power supply (VDDIOctrl) is at either 3.3 V, ±5%, or 2.5 V, ±5%.

Table 73. $\overline{\text{RESET}}$ AC Timing Specification

Symbol	Min	Typ	Max	Unit	Description	Conditions
T_{RESET}	100			ns	Reset assertion time	
T_{READY}		13	20	ms	Reset to SMI active time	If EEPROM is present, an additional 100ms is required

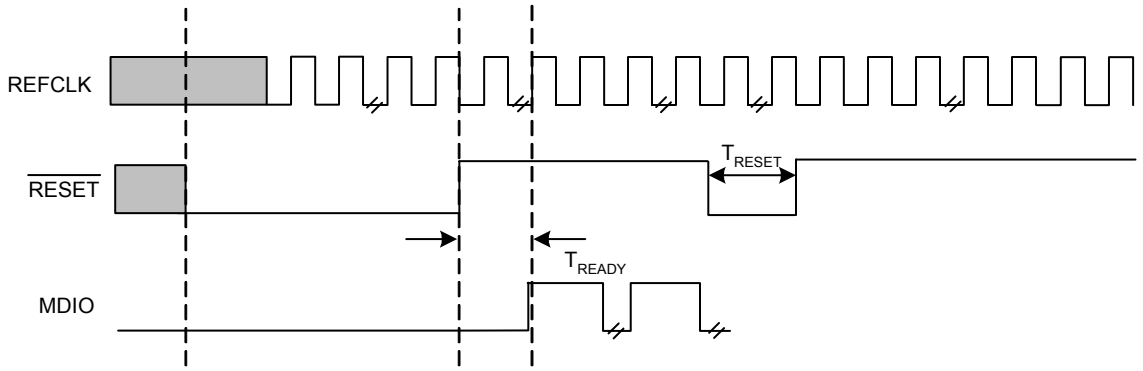

Figure 51. $\overline{\text{RESET}}$ AC Timing

31 Packaging Specifications

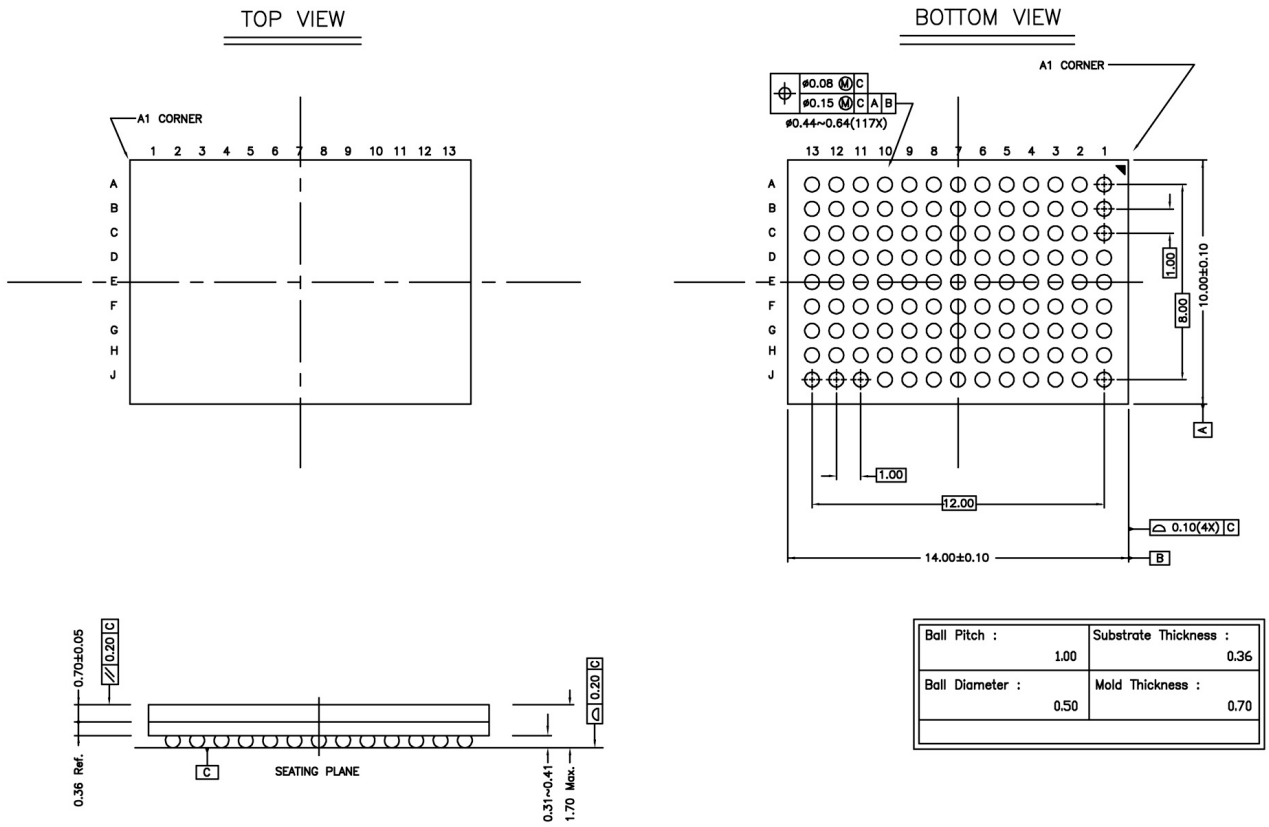

Figure 52. 117-ball 10x14mm LBGA Mechanical Specification

31.1 Package Moisture Sensitivity

Moisture sensitivity level ratings for Vitesse products comply with the joint IPC and JEDEC standard IPC/JEDEC J-STD-020. All Vitesse products are rated moisture sensitivity level 3 or better unless specified otherwise. For more information, see the IPC and JEDEC standard.

32 Ordering Information

Lead(Pb)-free products from Vitesse comply with the temperatures and profiles defined in the joint IPC and JEDEC standard IPC/JEDEC J-STD-020. For more information, see the IPC and JEDEC standard.

32.1 Devices

Part Number	Package Type	Description
VSC8211VW[1]	117 LBGA 1.0mm ball pitch 10mm x 14mm body	Single port, low-power, triple-speed PHY with GMII/MII, RGMII, TBI, RTBI, SGMII, and SerDes Interfaces.
VSC8211XVW	117 LBGA 1.0mm ball pitch 10mm x 14mm body	Lead(Pb)-free, single port, low-power, triple-speed PHY with GMII/MII, RGMII, TBI, RTBI, SGMII, and SerDes Interfaces.

[1] This device was previously available from Cicada Semiconductor Corporation (Cicada) as CIS8211-BLC. Cicada is now wholly owned by Vitesse Semiconductor Corporation, and the part number has been changed to reflect this.

33 Design Guidelines

These guidelines apply to Revision C of the VSC8211 silicon.

33.1 Required PHY Register Write Sequence

At initialization, a number of internal registers must be changed from their default values.

A series of register writes must be performed after device power-up or reset. These writes can be done using the EEPROM connected to the EEPROM Interface or by the Switch/Station Manager.

The required register writes are as follows:

2A30h to PHY Register 31.

0212h to PHY Register 8.

52B5h to PHY Register 31.

000Fh to PHY Register 2.

472Ah to PHY Register 1.

8FA4h to PHY Register 0.

2A30h to PHY Register 31.

0012h to PHY Register 8.

0000h to PHY Register 31.

33.2 Interoperability with Intel 82547EI Gigabit Ethernet MAC+PHY IC

Due to a non-standard startup-sequence in the Intel 82547EI MAC+PHY IC, the VSC8211 might take multiple attempts to establish link. The following PHY register write can be performed to avoid this issue:

0049h to MII Register 18.

33.3 SerDes Jitter

Under worst case conditions, total jitter performance may exceed the IEEE specifications for 1000BASE-X, as noted in the table below. In typical applications with robust PCB design practices, however, actual performance is typically better than the figures noted below.

Table 74. SerDes Jitter

Symbol	Min	Typ	Max	Unit	Parameter Description and Conditions
$J_{(TOTAL, TX)}$			290	ps	Worst case total transmit jitter in media converter applications.
$J_{(TOTAL, RX)}$			400	ps	Worst case total receive jitter tolerance in media converter applications.

33.4 100BASE-FX Initialization Script

The 100BASE-FX initialization script does the following:

- Initializes the copper section of DSP to support the 100BASE-FX mode
- Disables the pair swap option
- Sets 100BASE-X PCS into FX mode
- Forces the PHY into 100Mbps mode

The following script is provided as an attached text file so that you can copy it electronically. In Acrobat, double-click the attachment icon.

```
//--100BASE-FX initialization script for VSC8211.--//
phy_write( phynum(dec), regnum(dec), value(hex) );

phy_write(0, 31, 0x2a30);
phy_write(0,  8, 0x0212);
phy_write(0, 31, 0x52b5);
phy_write(0,  0, 0xa7fa);
phy_write(0,  2, 0x0012);
phy_write(0,  1, 0x3001);
phy_write(0,  0, 0x87fa);
phy_write(0, 31, 0x52b5);
phy_write(0,  0, 0xa240);
phy_write(0,  2, 0x0000);
phy_write(0,  1, 0x0001);
phy_write(0,  0, 0x8240);
phy_write(0, 31, 0x52b5);
phy_write(0,  0, 0xa70c);
phy_write(0,  2, 0x00e0);
phy_write(0,  1, 0x000d);
phy_write(0,  0, 0x870c);
phy_write(0, 31, 0x52b5);
phy_write(0,  0, 0xa70c);
phy_write(0,  2, 0x00e0);
phy_write(0,  1, 0x0000);
phy_write(0,  0, 0x870c);
phy_write(0, 31, 0x52b5);
phy_write(0,  0, 0xa258);
phy_write(0,  2, 0x0000);
phy_write(0,  1, 0x2140);
phy_write(0,  0, 0x8258);
phy_write(0, 31, 0x52b5);
phy_write(0,  0, 0xa258);
phy_write(0,  2, 0x0000);
phy_write(0,  1, 0x21c0);
phy_write(0,  0, 0x8258);
phy_write(0, 31, 0x52b5);
phy_write(0,  0, 0xa25a);
phy_write(0,  2, 0x0000);
phy_write(0,  1, 0x2940);
phy_write(0,  0, 0x825a);
phy_write(0, 31, 0x52b5);
phy_write(0,  0, 0xa25a);
phy_write(0,  2, 0x0000);
phy_write(0,  1, 0x29c0);
phy_write(0,  0, 0x825a);
```

```
phy_write(0, 31, 0x52b5);
phy_write(0,  0, 0xa25c);
phy_write(0,  2, 0x0000);
phy_write(0,  1, 0x3000);
phy_write(0,  0, 0x825c);
phy_write(0, 31, 0x52b5);
phy_write(0,  0, 0xa25c);
phy_write(0,  2, 0x0000);
phy_write(0,  1, 0x3000);
phy_write(0,  0, 0x825c);
phy_write(0, 31, 0x52b5);
phy_write(0,  0, 0xa25e);
phy_write(0,  2, 0x0000);
phy_write(0,  1, 0x38a0);
phy_write(0,  0, 0x825e);
phy_write(0, 31, 0x52b5);
phy_write(0,  0, 0xa25e);
phy_write(0,  2, 0x0000);
phy_write(0,  1, 0x3800);
phy_write(0,  0, 0x825e);
phy_write(0, 31, 0x52b5);
phy_write(0,  0, 0xafa2);
phy_write(0,  2, 0x0098);
phy_write(0,  1, 0x0000x;
phy_write(0,  0, 0x8fa2);
phy_write(0, 31, 0x52b5);
phy_write(0,  0, 0xafa2);
phy_write(0,  2, 0x009c);
phy_write(0,  1, 0x0000);
phy_write(0,  0, 0x8fa2);
phy_write(0, 31, 0x52b5);
phy_write(0,  0, 0xafa0);
phy_write(0,  2, 0x0013);
phy_write(0,  1, 0x1b00);
phy_write(0,  0, 0x8fa0);
phy_write(0, 31, 0x52b5);
phy_write(0,  0, 0xafa0);
phy_write(0,  2, 0x0013);
phy_write(0,  1, 0x9b00);
phy_write(0,  0, 0x8fa0);
phy_write(0, 31, 0x52b5);
phy_write(0,  0, 0xa708);
phy_write(0,  2, 0x000e);
phy_write(0,  1, 0x0004);
phy_write(0,  0, 0x8708);
phy_write(0, 31, 0x52b5);
phy_write(0,  0, 0xa708);
phy_write(0,  2, 0x000e);
phy_write(0,  1, 0x000c);
phy_write(0,  0, 0x8708);
phy_write(0, 31, 0x52b5);
phy_write(0,  0, 0xa708);
phy_write(0,  2, 0x000e);
phy_write(0,  1, 0x001c);
phy_write(0,  0, 0x8708);
phy_write(0, 31, 0x52b5);
phy_write(0,  0, 0xa708);
phy_write(0,  2, 0x000e);
phy_write(0,  1, 0x003c);
```

```
phy_write(0,  0, 0x8708);
phy_write(0, 31, 0x0000);
phy_write(0, 18, 0x0069);
phy_write(0, 31, 0x0000);
phy_write(0, 18, 0x7069);
phy_write(0, 31, 0x0000);
phy_write(0,  0, 0x2100);
```

34 Product Support

All support documents for the VSC8211 can be accessed on the Vitesse web site at *www.vitesse.com*. Access to some documents may require filing a non-disclosure agreement with Vitesse.

34.1 Available Documents and Application Notes

- IBIS Model
- OrCAD Symbol
- BSDL File
- Design and Layout Guidelines application note
- SimpliPHY'd Magnetics for EMI Control application note
- Using Jumbo Packets with SimpliPHYs application note
- UNH Test Report (requires NDA)

For additional application notes and information about reference designs using the VSC8211 PHY device, visit the Vitesse Web site at *www.vitesse.com*.

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For application support, latest technical literature, and locations of sales offices,
please visit our web site at
www.vitesse.com

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